COM EXPRESS CARRIER BOARD DESIGN GUIDE

Version 1.0
(January 2022)

iBASE

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Chapter 1
General Information

This design guide provides suggestions on designing IBASE COM-Express products including carrier boards and systems. For other carrier board schematic guidelines please refer to the full specification in the PICMG® COM Express® Carrier Board Design Guide.

This design guide is not a specification and should not be your sole reference. The guide is intended for electronics engineers and PCB layout engineers involved in the design of the COM Express Modules Carrier Boards. The schematic examples in this document are believed to be correct, however, no guarantee is given. The examples shown here have been taken from the designs that were already tested.

For any questions that you may have in the design of carrier boards, please contact IBASE sales representatives or engineers in your area.

1.1 ABOUT COM EXPRESS

COM Express is a highly integrated computer module that is integrated with the CPU, memory and I/O functions including USB, audio, graphics and Ethernet, which signals are mapped to two high-density, low-profile connectors at the bottom of the module.

COM Express uses a mezzanine concept, with a module inserted onto customized base boards. The module and base boards can be both upgraded to newer versions and to earlier-designed compatible versions. Common applications for COM Express modules are in various applications in the field of IoT, industrial automation, military, gaming, medical and transportation.

Chapter 2
COM Express Interfaces

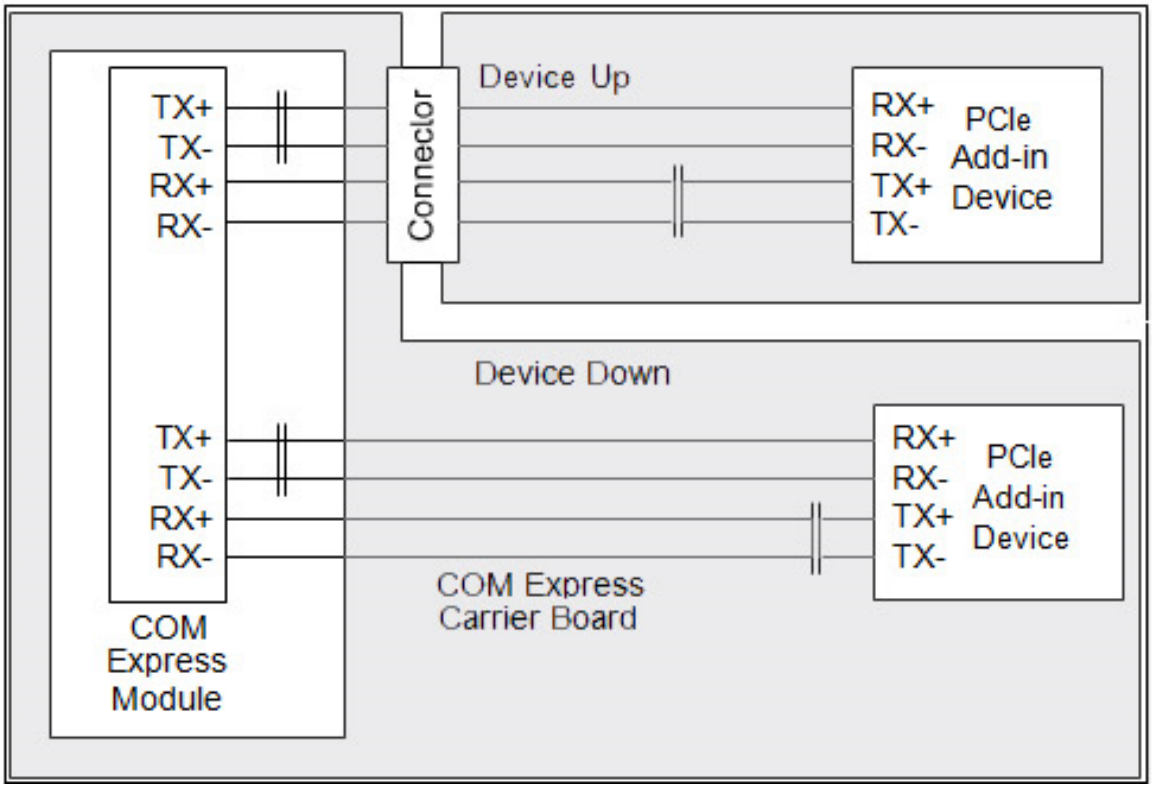
The information provided in this chapter includes:

- General Purpose PCIe Lanes
- PEG (PCI Express Graphics)
- Digital Display Interfaces
- LAN
- USB Ports
- USB 3.0
- SATA
- LVDS
- Embedded DisplayPort (eDP)
- VGA
- Digital Audio Interfaces
- LPC Bus – Low Pin Count Interface
- Serial Peripheral Interface Bus
- General Purpose I2C Bus Interface
- System Management Bus (SMBus)
- General Purpose Serial Interface
- CAN Interface
- Miscellaneous Signals
- PCI Bus
- IDE and CompactFlash (PATA)

2.1 General Purpose PCIe Lanes

2.1.1 Device Up / Device Down and PCIe Rx / Tx Coupling Capacitors

Figure 1: PCIe Rx Coupling Capacitors



The coupling caps for the Module PCIe TX lines are to be on the Module, as indicated in the COM Express specification.

2.1.2 Schematic Examples

Figure 2: PCI Express x1 Slot Example

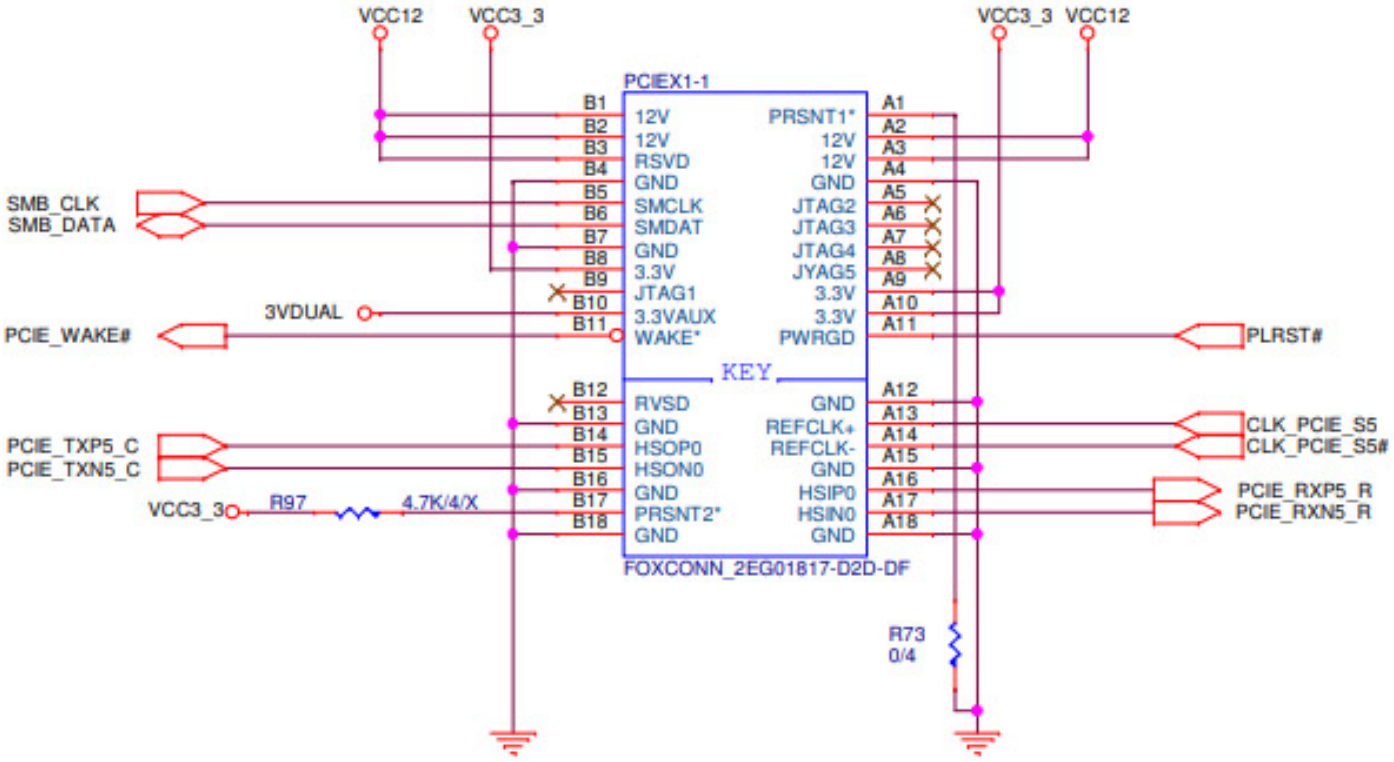


Figure 3: PCI Express x4 Slot Example

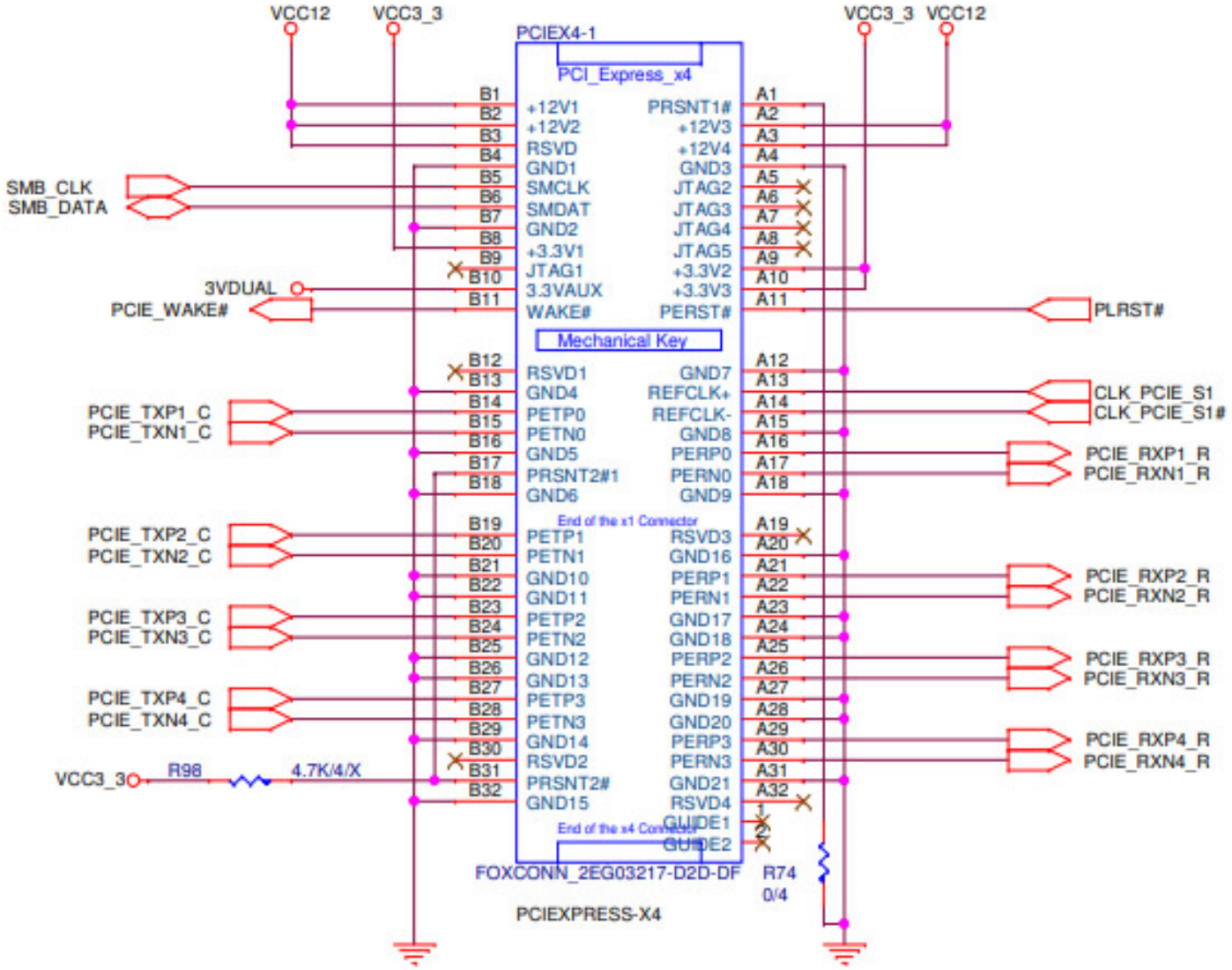
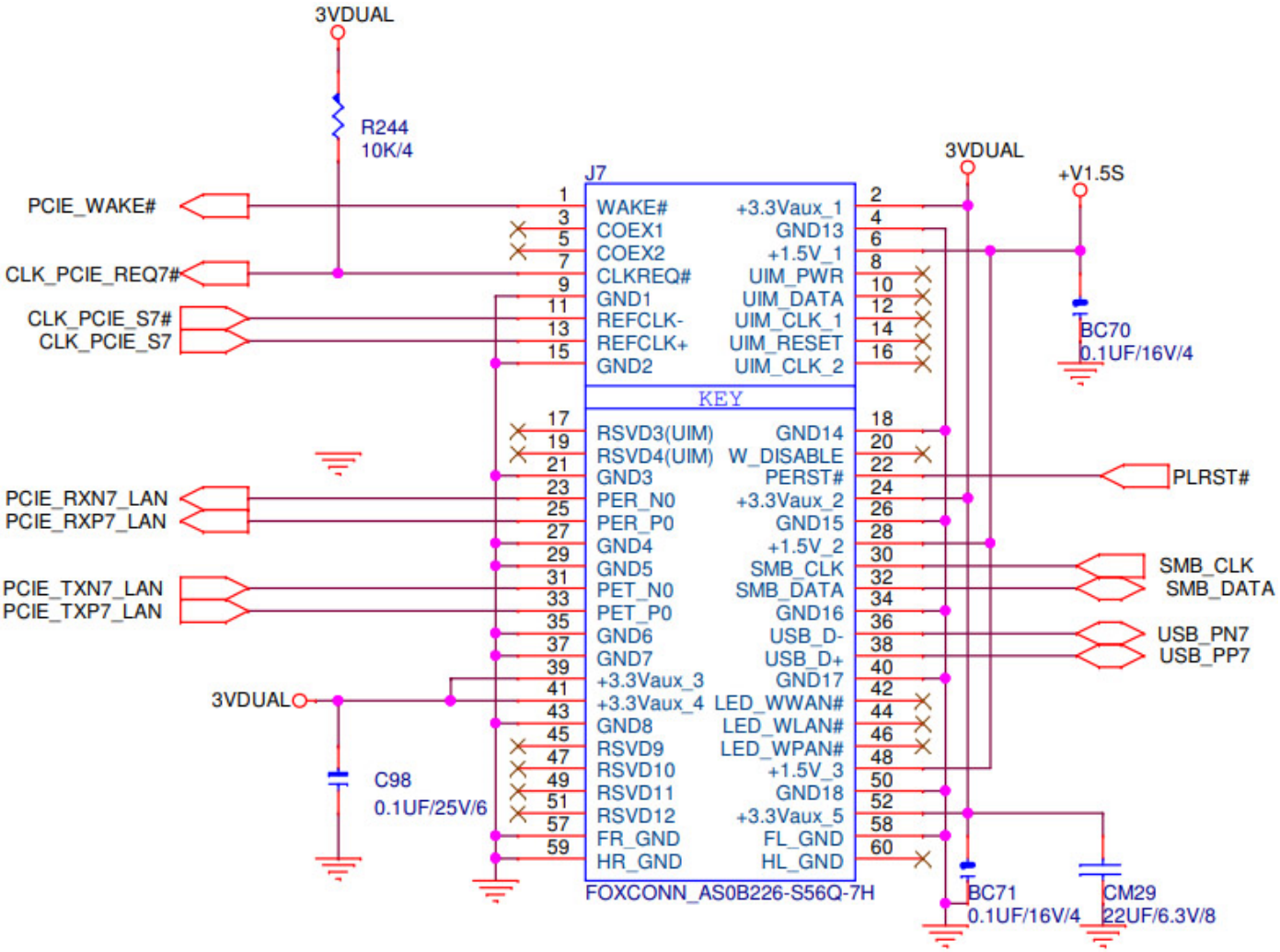


Figure 4: PCIe Mini Card Reference Circuitry



2.1.3 PCI Express Routing Considerations

New Carrier designs route the PCIe lanes with 85Ω (+/- 15%) differential impedance. Past designs for Gen1 and Gen2 signaling used 92Ω (+/- 10%) differential impedance. Gen1 designs used 100Ω (+/- 20%) differential impedance. New designs use 85Ω (+/- 15%) differential impedance for Gen1, Gen2 and Gen3 signaling. Route the traces as differential pairs, referenced to a continuous GND plane with a minimum of via transitions. PCIe pairs must have length-matched within a given pair (“intra-pair”). Different pairs do not need to be closely matched (“inter-pair”).

2.2 PEG (PCI Express Graphics)

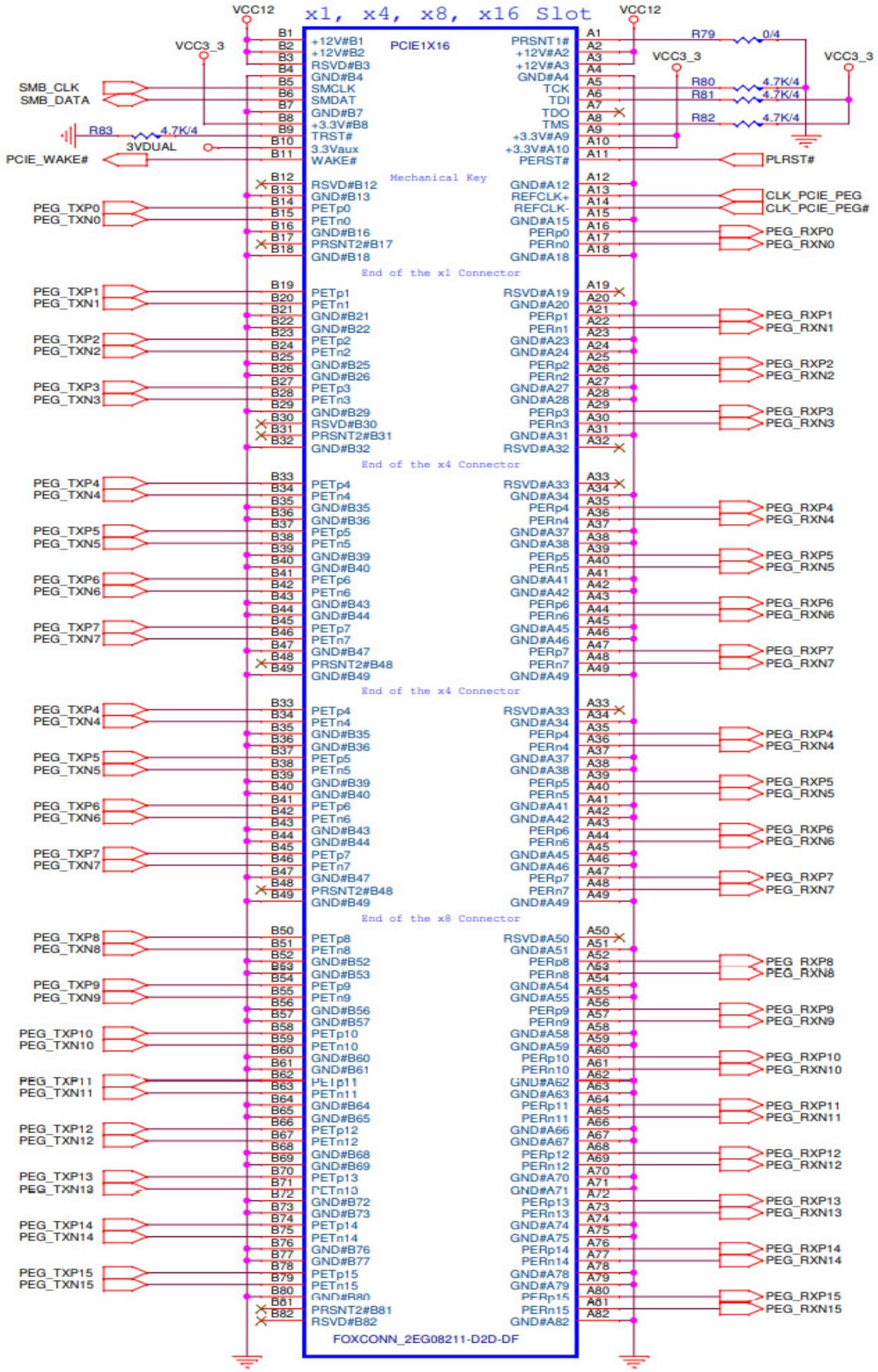
Table 1: PEG Signal Definitions

Signal	Pin#	Description	I/O	Remarks
PEG_RX0+ PEG_RX0-	C52 C53	PEG channel 0, Receive Input differential pair.	I PCIE	Type 2 SDVO_TVCLKIN+ Shared with: SDVO_TVCLKIN-
PEG_TX0+ PEG_TX0-	D52 D53	PEG channel 0, Transmit Output differential pair.	O PCIE	Type 2 SDVOB_RED+ Shared with: SDVOB_RED-
PEG_RX1+ PEG_RX1-	C55 C56	PEG channel 1, Receive Input differential pair.	I PCIE	Type 2 SDVOB_INT+ Shared with: SDVOB_INT-
PEG_TX1+ PEG_TX1-	D55 D56	PEG channel 1, Transmit Output differential pair.	O PCIE	Type 2 SDVOB_GRN+ Shared with: SDVOB_GRN-
PEG_RX2+ PEG_RX2-	C58 C59	PEG channel 2, Receive Input differential pair.	I PCIE	Type 2 SDVO_FLDSTALL+ Shared with: SDVO_FLDSTALL-
PEG_TX2+ PEG_TX2-	D58 D59	PEG channel 2, Transmit Output differential pair.	O PCIE	Type 2 SDVOB_BLU+ Shared with: SDVOB_BLU-
PEG_RX3+ PEG_RX3-	C61 C62	PEG channel 3, Receive Input differential pair.	I PCIE	
PEG_TX3+ PEG_TX3-	D61 D62	PEG channel 3, Transmit Output differential pair.	O PCIE	Type 2 SDVOB_CK+ Shared with: SDVOB_CK-
PEG_RX4+ PEG_RX4-	C65 C66	PEG channel 4, Receive Input differential pair.	I PCIE	
PEG_TX4+ PEG_TX4-	D65 D66	PEG channel 4, Transmit Output differential pair.	O PCIE	Type 2 SDVOC_RED+ Shared with: SDVOC_RED-
PEG_RX5+ PEG_RX5-	C68 C69	PEG channel 5, Receive Input differential pair.	I PCIE	Type 2 SDVOC_INT+ Shared with: SDVOC_INT-
PEG_TX5+ PEG_TX5-	D68 D69	PEG channel 5, Transmit Output differential pair.	O PCIE	Type 2 SDVOC_GRN+ Shared with: SDVOC_GRN-
PEG_RX6+ PEG_RX6-	C71 C72	PEG channel 6, Receive Input differential pair.	I PCIE	
PEG_TX6+ PEG_TX6-	D71 D72	PEG channel 6, Transmit Output differential pair.	O PCIE	Type 2 SDVOC_BLU+ Shared with SDVOC_BLU-
PEG_RX7+ PEG_RX7-	C74 C75	PEG channel 7, Receive Input differential pair.	I PCIE	
PEG_TX7+ PEG_TX7-	D74 D75	PEG channel 7, Transmit Output differential pair.	O PCIE	Type 2 SDVOC_CK+ Shared with SDVOC_CK-
PEG_RX8+ PEG_RX8-	C78 C79	PEG channel 8, Receive Input differential pair.	I PCIE	
PEG_TX8+ PEG_TX8-	D78 D79	PEG channel 8, Transmit Output differential pair.	O PCIE	
PEG_RX9+ PEG_RX9-	C81 C82	PEG channel 9, Receive Input differential pair.	I PCIE	
PEG_TX9+ PEG_TX9-	D81 D82	PEG channel 9, Transmit Output	O PCIE	
PEG_RX10+ PEG_RX10-	C85 C86	PEG channel 10, Receive Input differential	I PCIE	
PEG_TX10+ PEG_TX10-	D85 D86	PEG channel 10, Transmit Output	O PCIE	
PEG_RX11+ PEG_RX11-	C88 C89	PEG channel 11, Receive Input differential	I PCIE	
PEG_TX11+ PEG_TX11-	D88 D89	PEG channel 11, Transmit Output	O PCIE	

Signal	Pin#	Description	I/O	Remarks
PEG_RX12+ PEG_RX12-	C91 C92	PEG channel 12, Receive Input differential pair.	I PCIE	
PEG_TX12+ PEG_TX12-	D91 D92	PEG channel 12, Transmit Output differential pair.	O PCIE	
PEG_RX13+ PEG_RX13-	C94 C95	PEG channel 13, Receive Input differential pair.	I PCIE	
PEG_TX13+ PEG_TX13-	D94 D95	PEG channel 13 Transmit Output differential pair.	O PCIE	
PEG_RX14+ PEG_RX14-	C98 C99	PEG channel 14, Receive Input differential pair.	I PCIE	
PEG_TX14+ PEG_TX14-	D98 D99	PEG channel 14, Transmit Output differential pair.	O PCIE	
PEG_RX15+ PEG_RX15-	C101 C102	PEG channel 15, Receive Input differential pair.	I PCIE	
PEG_TX15+ PEG_TX15-	D101 D102	PEG channel 15, Transmit Output differential pair.	O PCIE	
SDVO_I2C_CLK	D73	I2C based control signal (clock) for SDVO device.	O 2.5V CMOS	SDVO enabled if this line is pulled up to 2.5V on Carrier or on ADD2 (Type 2 only)
SDVO_I2C_DATA	C73	I2C based control signal (data) for SDVO device	I/O 2.5V OD CMOS	SDVO enabled if this line is pulled up to 2.5V on Carrier or on ADD2 (Type 2 only)
PEG_LANE_RV#	D54	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I 3.3V CMOS	
PEG_ENABLE#	D97	PEG enable function. Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface.	I 3.3V CMOS	Type 2 only
PCIE_CLK_REF+ PCIE_CLK_REF-	A88 A89	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes	O CMOS	COM Express only allocates a single reference clock

2.2.1 Reference Schematics

Figure 5: x1, x4, x8, x16 Slot



2.3 Digital Display Interfaces

Module Types 6 and 10 use Digital Display Interfaces (DDI) to provide DisplayPort, HDMI/DVI, and SDVO interfaces. Type 10 Modules can contain a single DDI (DDI[0]) that can support DisplayPort, HDMI/DVI, and SDVO. Type 6 Modules can contain up to 3 DDIs (DDI[1:3]) of which DDI[1:3] can support DisplayPort, HDMI/DVI and DDI[1] can support DisplayPort, HDMI/DVI, and SDVO. The main difference is that SDVO is only supported on DDI[0] for Type 10 Modules and DDI[1] for Type 6 Modules.

2.3.1 DisplayPort / HDMI / DVI

Type 10 offers up to one DisplayPort interface and Type 6 Modules up to 3 DisplayPort interfaces. Both implementations are similar, so only one reference schematic is necessary to show Carrier Board implementation.

Each DisplayPort interface consists of 4 differential lanes, 1 auxiliary lane and 1 hot-plug-detect signal. The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels.

Table 2: Display Port / HDMI / DVI Pin-out of Type 10 and Type 6

COM Express Pin Name	DDI0 Type 10	DDI1 Type 6	DDI2 Type 6	DDI3 Type 6	Function (DDIX)	Function (DDIX) HDMI / DVI
DDIX_PAIR0+	B71	D26	D39	C39	DPX_LANE0+	TMDSX_DATA2+
DDIX_PAIR0-	B72	D27	D40	C40	DPX_LANE0-	TMDSX_DATA2-
DDIX_PAIR1+	B73	D29	D42	C42	DPX_LANE1+	TMDSX_DATA1+
DDIX_PAIR1-	B74	D30	D43	C43	DPX_LANE1-	TMDSX_DATA1-
DDIX_PAIR2+	B75	D32	D46	C46	DPX_LANE2+	TMDSX_DATA0+
DDIX_PAIR2-	B76	D33	D47	C47	DPX_LANE2-	TMDSX_DATA0-
DDIX_PAIR3+	B81	D36	D49	C49	DPX_LANE3+	TMDSX_CLK+
DDIX_PAIR3-	B82	D37	D50	C50	DPX_LANE3-	TMDSX_CLK-
DDIX_HPD	B89	C24	D44	C44	DPX_HPD	HDMIX_HPD
DDIX_CTRLCLK_AUX	B98	D15	C32	C36	DPX_AUX+	HDMIX_CTRLCLK
DDIX_CTRLDATA_AU	B99	D16	C33	C37	DPX_AUX-	HDMIX_CTRLDATA
DDIX_DDC_AUX_SEL	B95	D34	C34	C38		

2.3.1.1 Reference Schematic

Figure 6: DisplayPort Reference Schematics

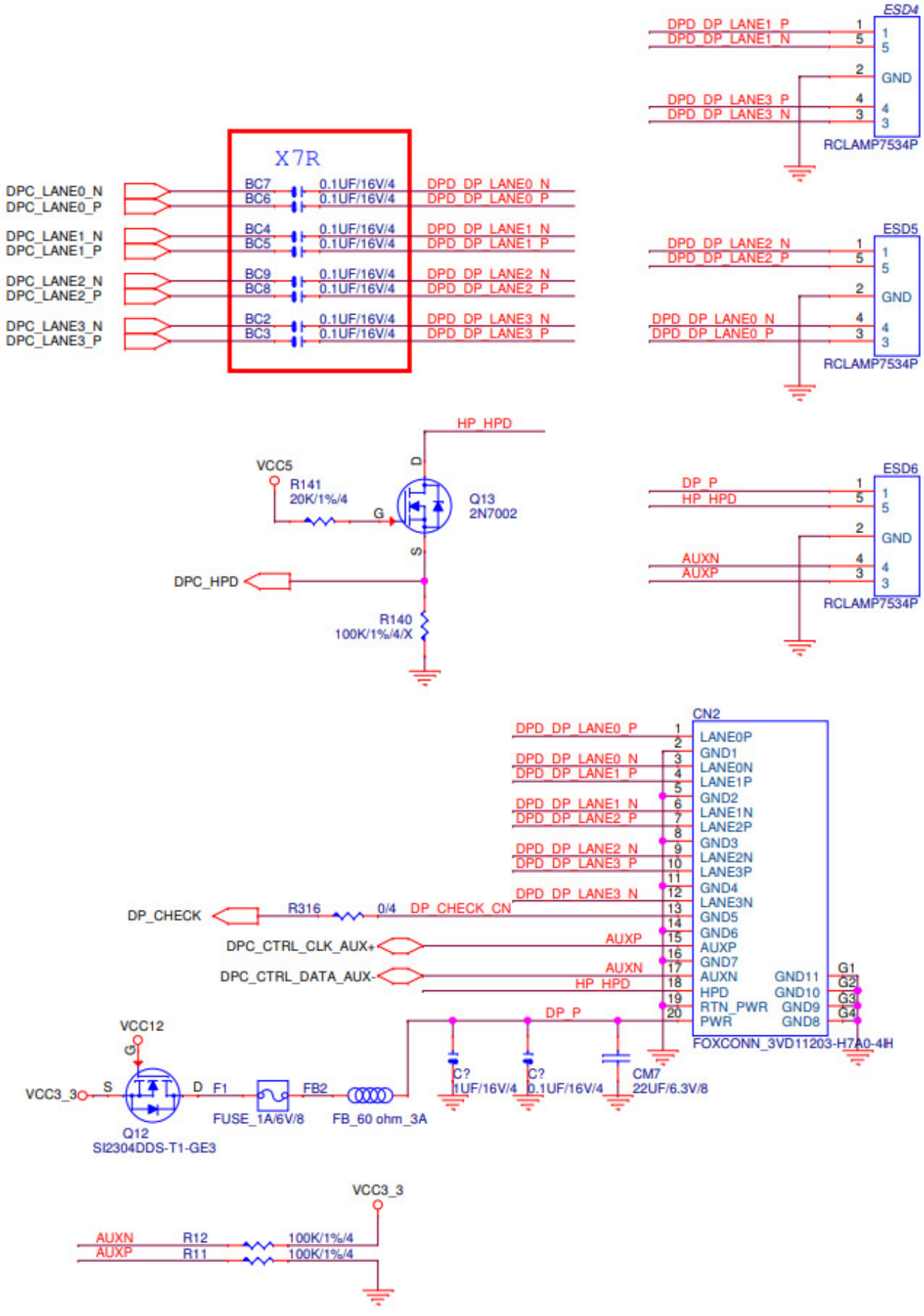


Figure 7: HDMI Example (1)

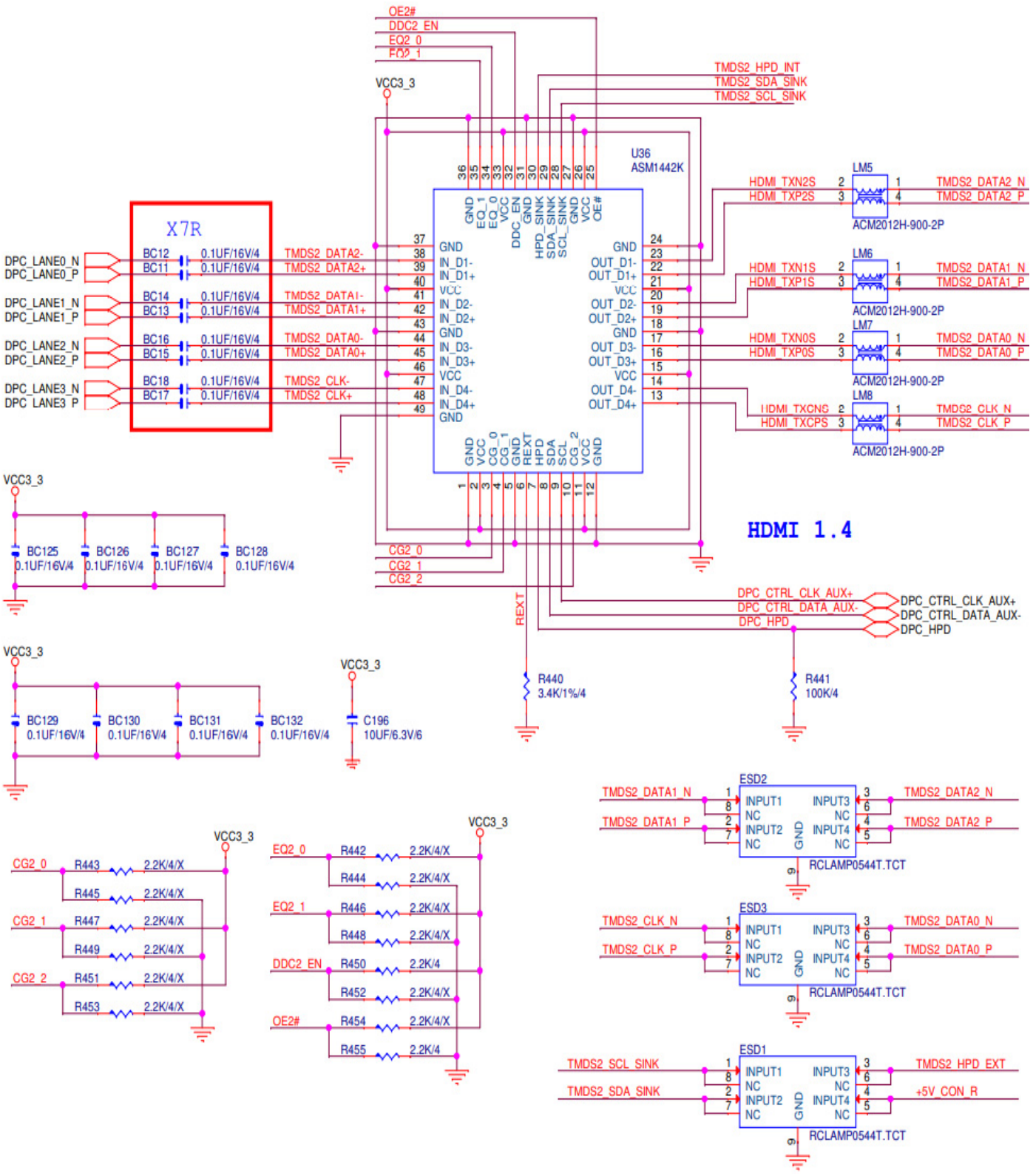


Figure 7: HDMI Example (2)

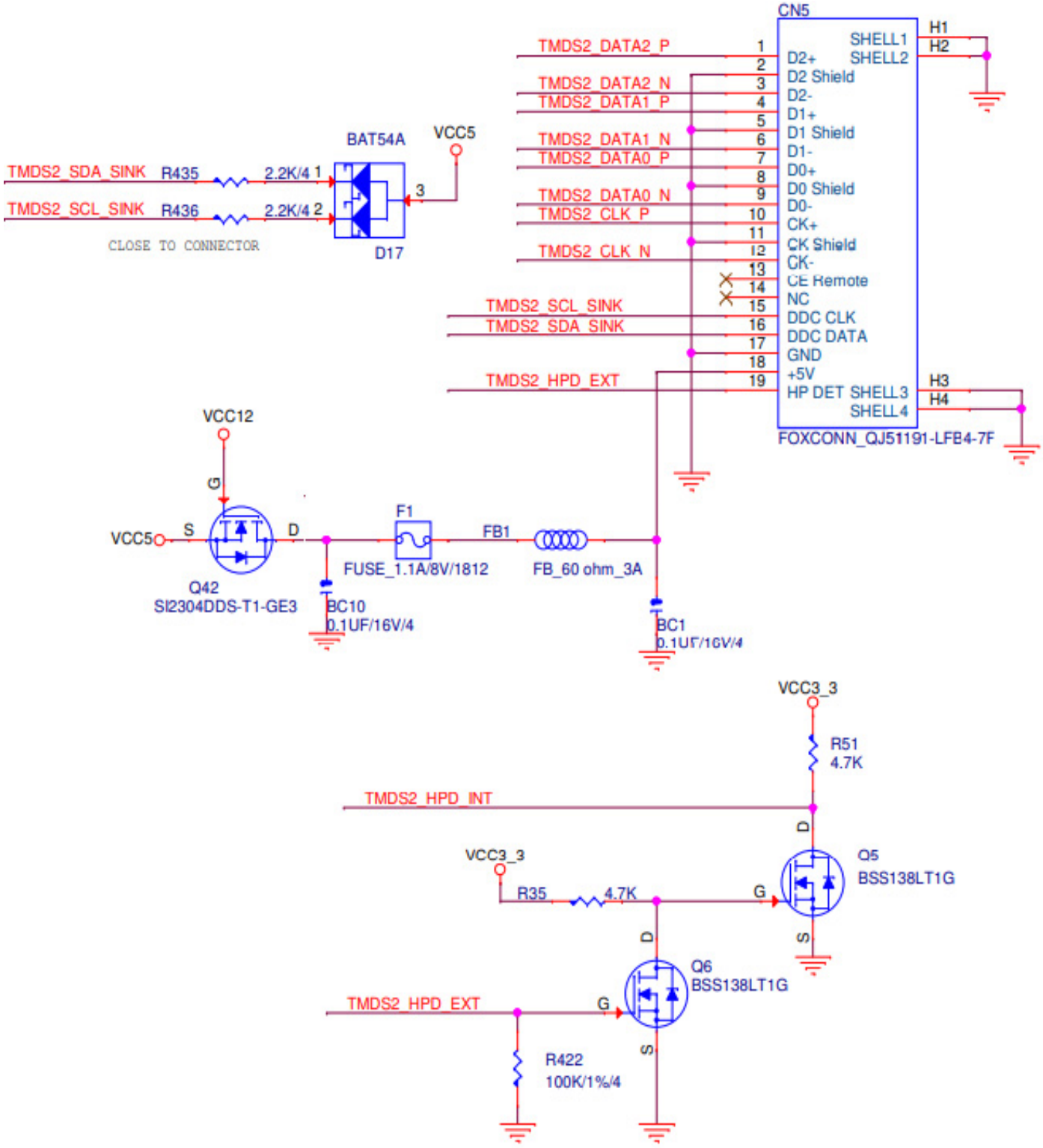


Figure 8: DVI Example (1)

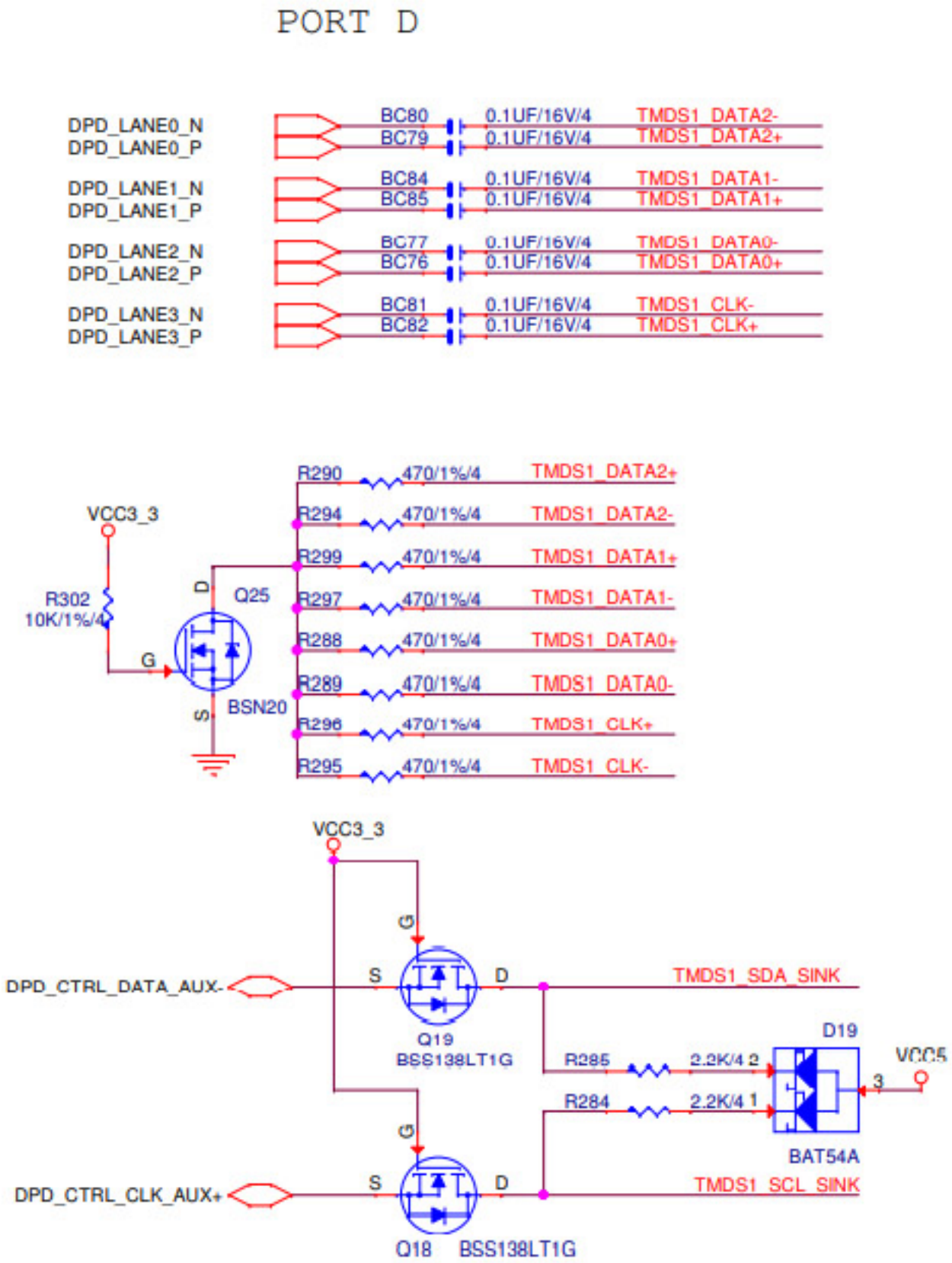


Figure 8: DVI Example (2)

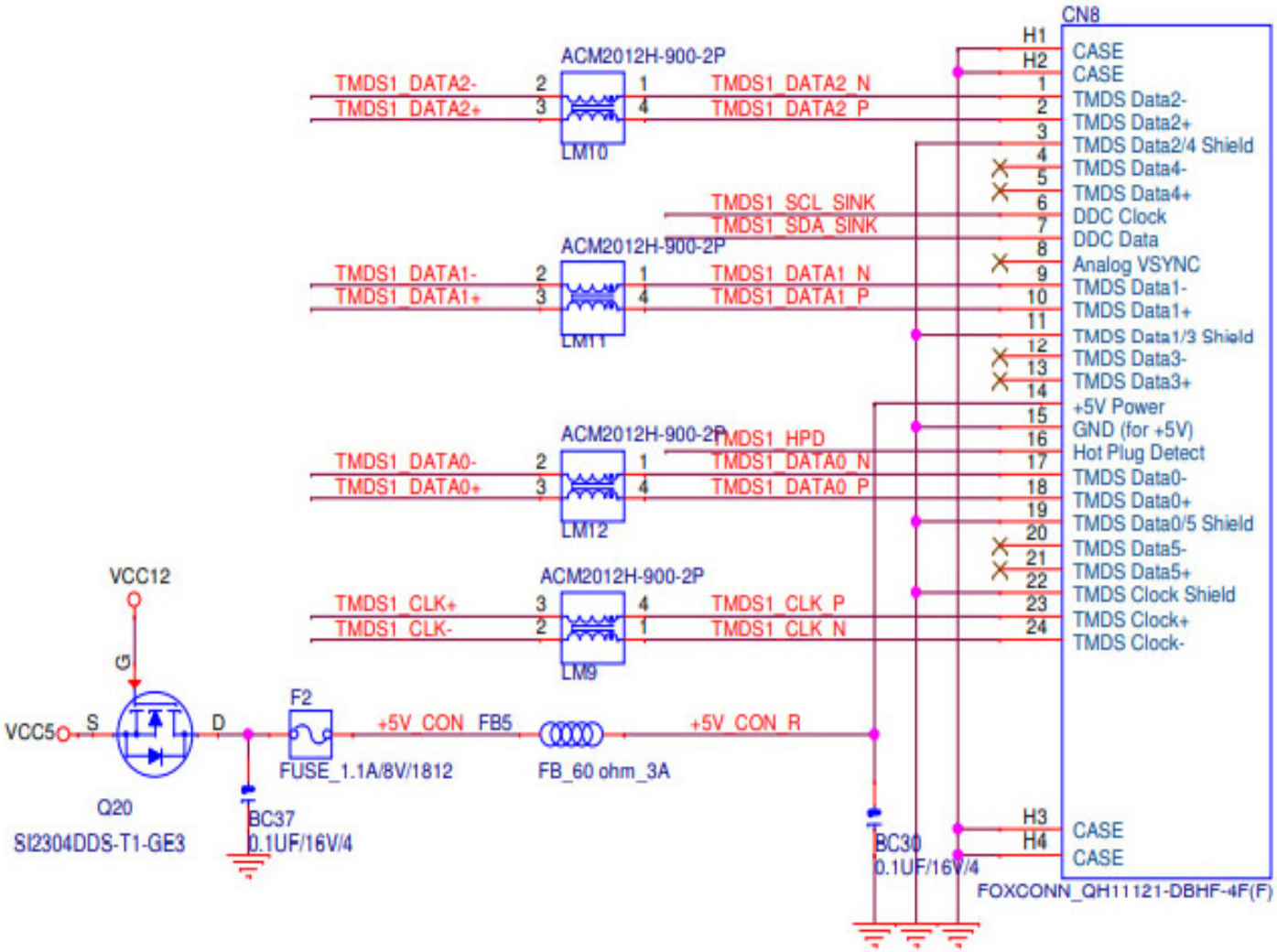
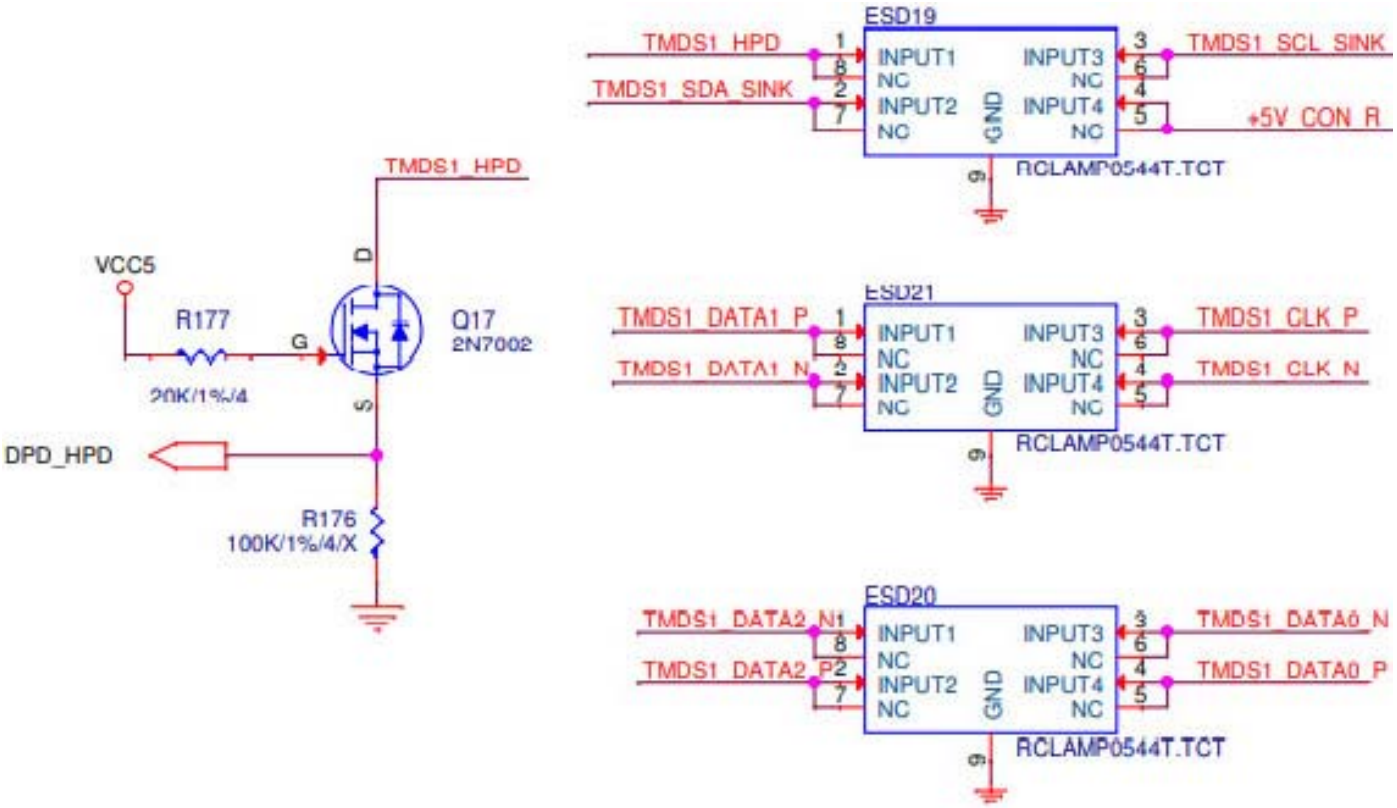


Figure 8: DVI Example (3)



2.3.1.2 Routing Considerations

For the DisplayPort interconnection between the COM Express Module and the DisplayPort connector or the level shifter, refer to the COM Express Carrier Design Guide, Rev. 2.0 / December 6, 2013, Section 6.5.6 'DisplayPort Trace Routing Guidelines' on page 186 for details.

The DVI and HDMI interface are based on the differential signaling method TMDS. The TDMS differential signals between the level shifter and the DVI connector have to be routed in pairs with a differential impedance of 100Ω. The length of the differential signals must be kept close. The maximum length difference must be within 100mils for any of the pairs relative to each other. Pair to pair spacing be over 2x the trace width to reduce trace-to-trace couplings. Having wider gaps between differential pair DVI traces will reduce noise coupling. Ground should not be placed adjacent to the DVI traces on the same layer. There should be at least 30mils between the DVI trace and any ground on the same layer.

2.3.2 SDVO

2.3.2.1 Signal Definitions

Type 6 Modules allow one SDVO port on DDI[1]. The DDI port needs to be configured to be used as SDVO usually via the Module's BIOS.

On Type 2 Modules the pins for SDVO ports B and C are shared with the PEG port.

Table 3: SDVO Port Configuration

	SDVO Port B	SDVO Port C
Device Type	Selectable in BIOS Setup Program.	Selectable in BIOS Setup Program.
I²C Address	0111 000x	0111 001x
I²C Bus	SDVO I²C GPIO pins	SDVO I²C GPIO pins
DDC Bus	SDVO I²C GPIO pins	SDVO I²C GPIO pins

2.3.2.2 Reference Schematics

Figure 9: SDVO to DVI Transmitter Example
Please refer to:
PICMG COM Express Carrier Board Design Guide
Rev. 2.0 / December 6, 2013
Page 59, Figure 22: DVI Example

2.3.2.3 Routing Considerations

DVI is based on the differential signaling method TDMS. The TDMS differential signals between the SDVO to DVI transmitter and the DVI connector have to be routed in pairs with a differential impedance of 100Ω. The length of the differential signals must be kept close. The length difference must within 100mils for any of the pairs relative to each other. Spacing between the differential pair traces should be over 2x the trace width to reduce trace-to-trace couplings. Having wider gaps between differential pair DVI traces will reduce noise coupling. Ground should not be placed adjacent to the DVI traces on the same layer. Keep a distance of at least 30mils between the DVI trace and any ground on the same layer.

2.4 LAN

In general, COM Express Modules provide at least one LAN port. The 8-wire 10/100/1000BASE-T Gigabit Ethernet interface compliant to the IEEE 802.3-2005 specification is the preferred interface for this port, with the COM Express Module PHY responsible for implementing auto-negotiation of 10/100BASE-TX vs 10/100/1000BASE-T operation. The carrier may also support a 4-wire 10/100BASE-TX interface from the COM Express Module on an exception basis.

2.4.1 Signal Definitions

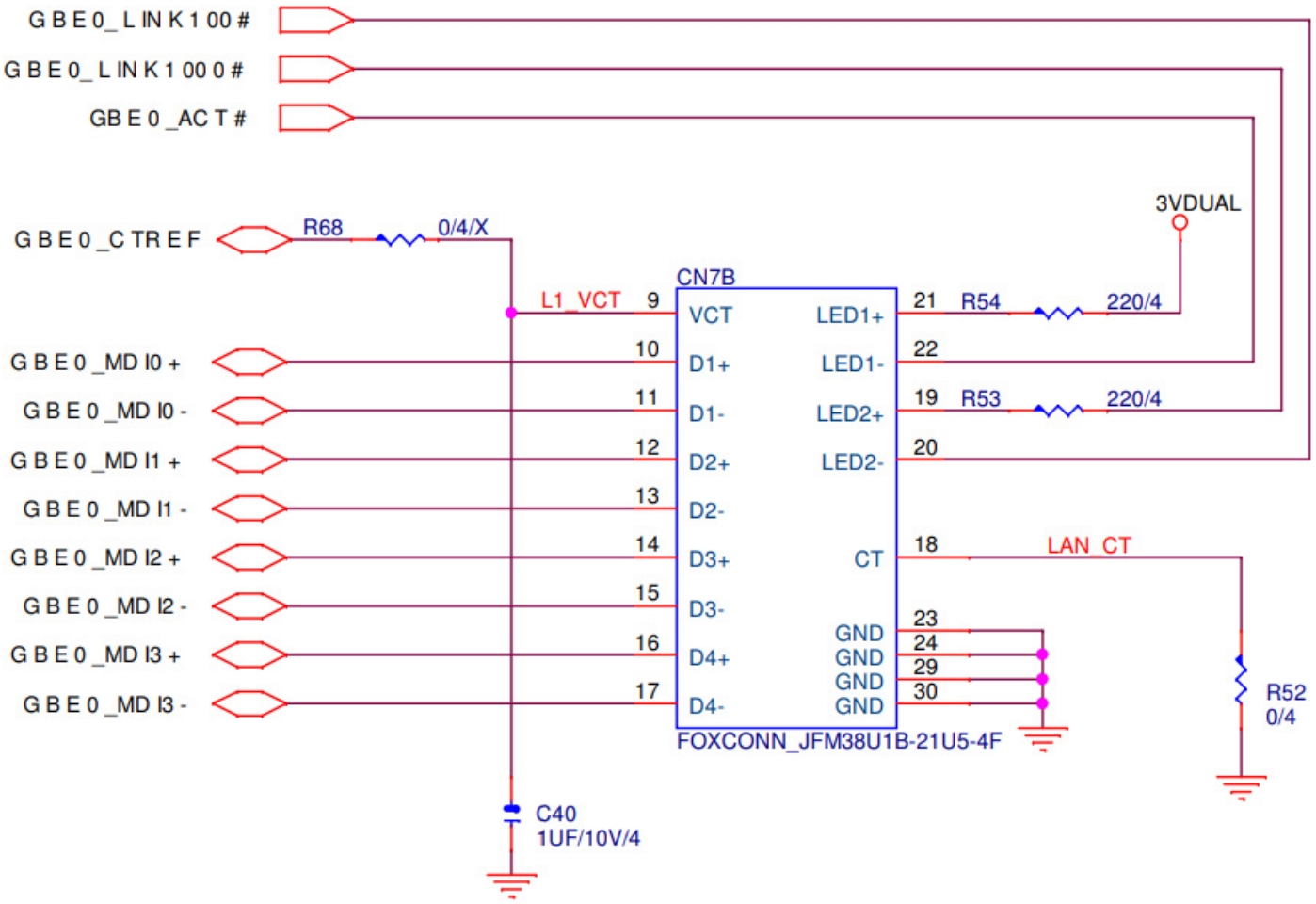
The LAN interface of the COM Express Module has 4 pairs of low voltage differential pair signals designated from 'GBE0_MDI0' (+ and -) to 'GBE0_MDI3' (+ and -) plus additional control signals for link activity indicators. The signals can connect to a 10/100/1000BASE-T RJ45 connector with integrated or external isolation magnetics on the Carrier Board. The corresponding LAN differential pair and control signals can be found on rows A and B of the Module's connector, as listed below.

Table 4: LAN Interface Signal Descriptions

Signal	Pin#	Description	I/O	Remarks
GBE0_MDI0+ GBE0_MDI0-	A13 A12	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE	This signal pair is used for all modes.
GBE0_MDI1+ GBE0_MDI1-	A10 A9	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE	This signal pair is used for all modes.
GBE0_MDI2+ GBE0_MDI2-	A7 A6	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE	This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_MDI3+ GBE0_MDI3-	A3 A2	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE	This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_CTREF	A14	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.	REF	
GBE0_LINK#	A8	Ethernet controller 0 link indicator, active low.	O 3.3V Suspend OD CMOS	
GBE0_LINK100#	A4	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3V Suspend OD CMOS	
GBE0_LINK1000#	A5	Ethernet controller 0 1000Mbit/sec link indicator, active low.	O 3.3V Suspend OD CMOS	
GBE0_ACT#	B2	Ethernet controller 0 activity indicator, active low.	O 3.3V Suspend OD CMOS	

2.4.2 Reference Schematics

Figure 10: Magnetics Integrated Into RJ-45 Receptacle



2.4.3 Routing Considerations

The 8-wire PHY / MDI circuit is required to meet a specific waveform template and associated signal integrity requirements defined in the IEEE 802.3-2005 specification. Routing rules should be observed on the Carrier Board.

The four status signals driven by the COM Express Module to the Carrier Board are low frequency signals that do not have any signal integrity or trace routing requirements beyond the accepted design practices.

2.5 USB Ports

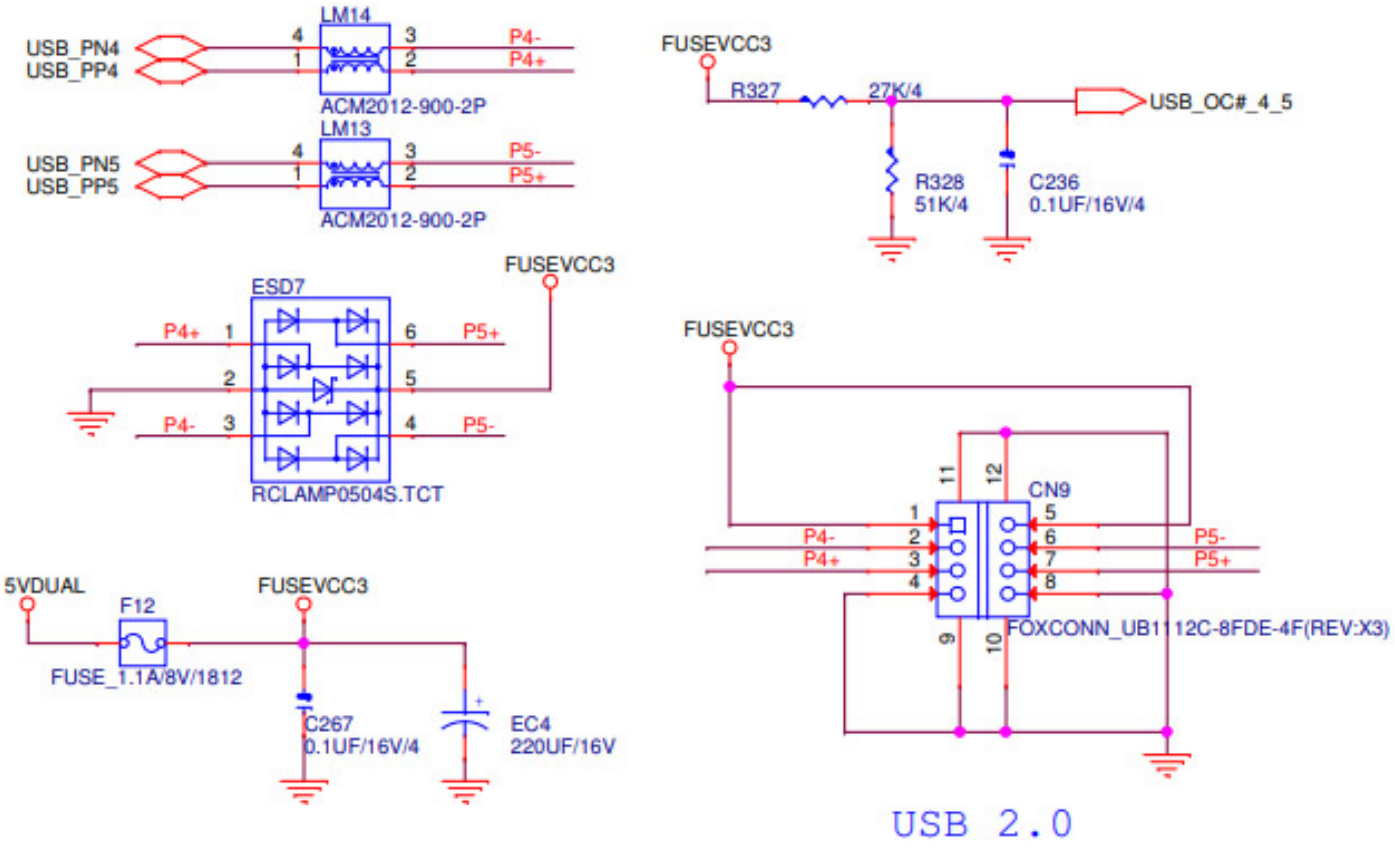
2.5.1 Signal Definitions

Table 5: USB Signal Description

Signal	Pin	Description	I/O	Remarks
USB0+	A46	USB Port 0, data + or D+	I/O USB	mandatory on Module
USB0-	A45	USB Port 0, data - or D-	I/O USB	mandatory on Module
USB1+	B46	USB Port 1, data + or D+	I/O USB	mandatory on Module
USB1-	B45	USB Port 1, data - or D-	I/O USB	mandatory on Module
USB2+	A43	USB Port 2, data + or D+	I/O USB	mandatory on Module
USB2-	A42	USB Port 2, data - or D-	I/O USB	mandatory on Module
USB3+	B43	USB Port 3, data + or D+	I/O USB	mandatory on Module
USB3-	B42	USB Port 3, data - or D-	I/O USB	mandatory on Module
USB4+	A40	USB Port 4, data + or D+	I/O USB	optional on Module
USB4-	A39	USB Port 4, data - or D-	I/O USB	optional on Module
USB5+	B40	USB Port 5, data + or D+	I/O USB	optional on Module
USB5-	B39	USB Port 5, data - or D-	I/O USB	optional on Module
USB6+	A37	USB Port 6, data + or D+	I/O USB	optional on Module
USB6-	A36	USB Port 6, data - or D-	I/O USB	optional on Module
USB7+	B37	USB Port 7, data + or D+	I/O USB	optional on Module
USB7-	B36	USB Port 7, data - or D-	I/O USB	optional on Module
USB_0_1_OC#	B44	USB over-current sense, USB ports 0 and 1.	I 3.3V CMOS	optional on Module
USB_2_3_OC#	A44	USB over-current sense, USB ports 2 and 3.	I 3.3VCMOS	optional on Module
USB_4_5_OC#	B38	USB over-current sense, USB ports 4 and 5.	I 3.3V CMOS	optional on Module
USB_6_7_OC#	A38	USB over-current sense, USB ports 6 and 7.	I 3.3V CMOS	optional on Module

2.5.2 Reference Schematics

Figure 11: USB Reference Design



2.5.3 Routing Considerations

Route USB signals as differential pairs, with a 90-Ω differential impedance and a 45-Ω, single-ended impedance. A USB pair is routed on a single layer adjacent to a ground plane.
USB pairs should not cross plane splits. Limit layer transitions to a minimum. Reference USB pairs to a power plane when necessary. The power plane must be well-bypassed.

2.6 USB 3.0

2.6.1 Signal Definitions

Table 5: USB 2.0 Differential Lines

Signal	Pins	Pins	Description	I/O
USB0+	A46	A46	USB Port 0, data + or D+	I/O USB
USB0-	A45	A45	USB Port 0, data - or D-	I/O USB
USB1+	B46	B46	USB Port 1, data + or D+	I/O USB
USB1-	B45	B45	USB Port 1, data - or D-	I/O USB
USB2+	A43		USB Port 2, data + or D+	I/O USB
USB2-	A42		USB Port 2, data - or D-	I/O USB
USB3+	B43		USB Port 3, data + or D+	I/O USB
USB3-	B42		USB Port 3, data - or D-	I/O USB

Table 6: USB Overcurrent Protection lines

Signal	Pins	Pins	Description	I/O
USB_0_1_OC#	B44	B44	USB over-current sense, USB channels 0 and 1.	I CMOS
USB_2-3_OC#	A44		USB over-current sense, USB channels 2 and 3.	I CMOS

Table 7: USB 3.0 Differential Lines

Signal	Pins	Pins	Description	I/O
USB_SSTX0+	D4	B23	USB Port 0, SuperSpeed TX +	O PCIE
USB_SSTX0-	D3	B22	USB Port 0, SuperSpeed TX -	O PCIE
USB_SSTX1+	D7	B26	USB Port 1, SuperSpeed TX +	O PCIE
USB_SSTX1-	D6	B25	USB Port 1, SuperSpeed TX -	O PCIE
USB_SSTX2+	D10		USB Port 2, SuperSpeed TX +	O PCIE
USB_SSTX2-	D9		USB Port 2, SuperSpeed TX -	O PCIE
USB_SSTX3+	D13		USB Port 3, SuperSpeed TX +	O PCIE
USB_SSTX3-	D12		USB Port 3, SuperSpeed TX -	O PCIE
USB_SSRX0+	C4	A23	USB Port 0, SuperSpeed RX +	I PCIE
USB_SSRX0-	C3	A22	USB Port 0, SuperSpeed RX -	I PCIE
USB_SSRX1+	C7	A26	USB Port 1, SuperSpeed RX +	I PCIE
USB_SSRX1-	C6	A25	USB Port 1, SuperSpeed RX -	I PCIE
USB_SSRX2+	C10		USB Port 2, SuperSpeed RX +	I PCIE
USB_SSRX2-	C9		USB Port 2, SuperSpeed RX -	I PCIE
USB_SSRX3+	C13		USB Port 3, SuperSpeed RX +	I PCIE
USB_SSRX3-	C12		USB Port 3, SuperSpeed RX -	I PCIE

2.6.2 Reference Schematics

Figure 12: USB 3.0 Example (1)

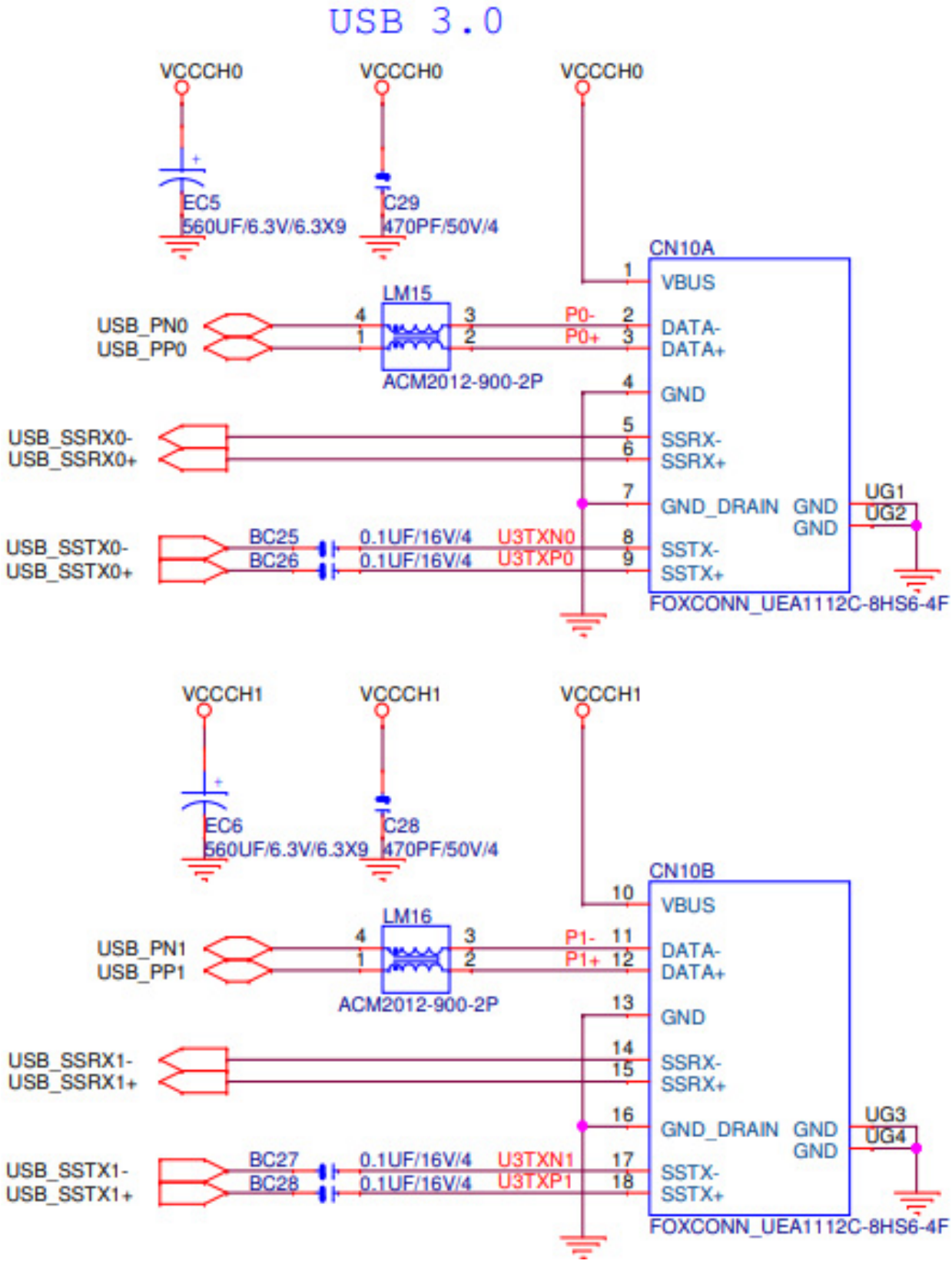
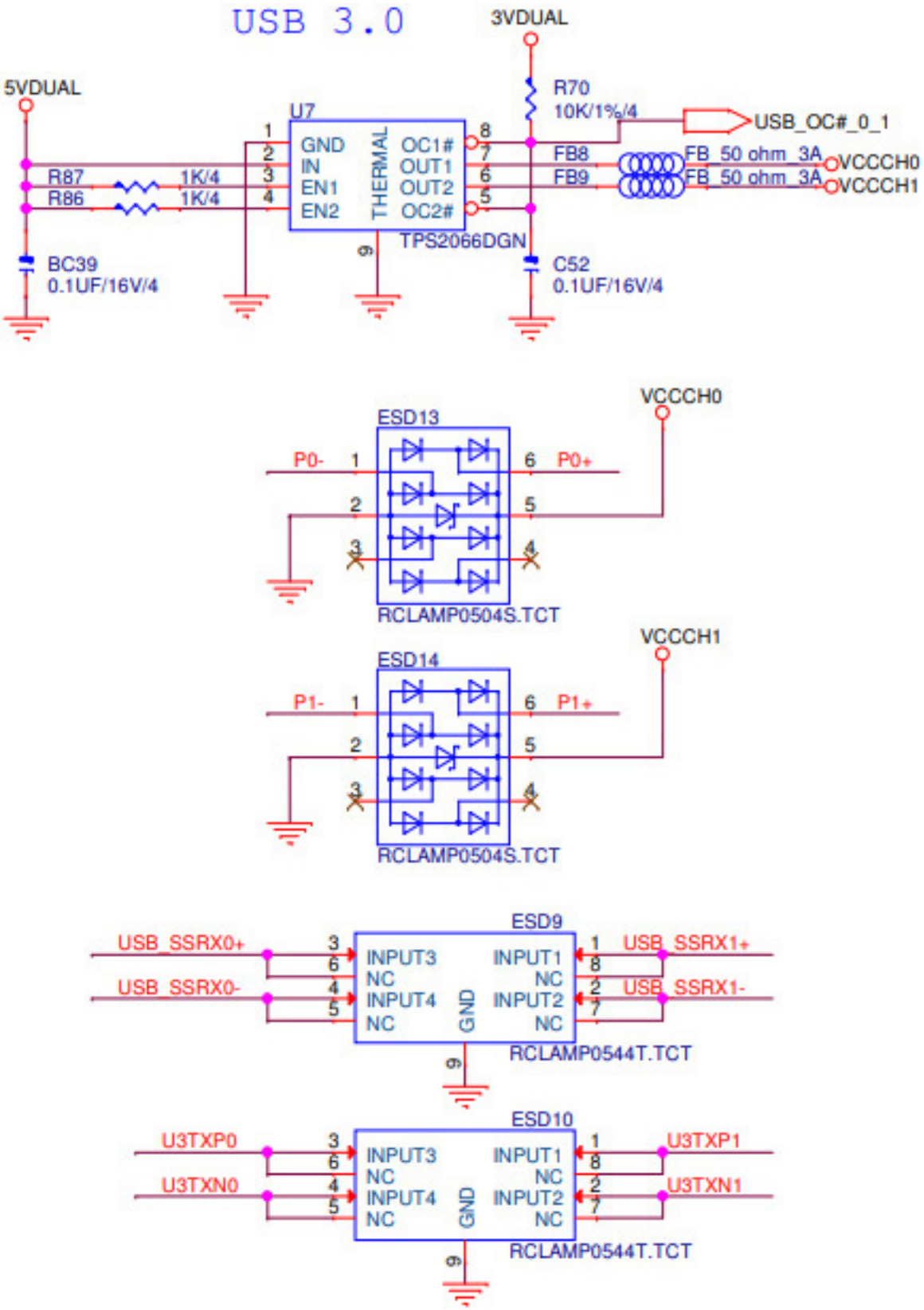


Figure 12: USB 3.0 Example (2)



2.6.3 Routing Considerations

Route USB data signals as differential pairs, with a 90-Ω differential impedance and a 45-Ω, single-ended impedance. Route USB SuperSpeed signals as differential pairs, with an 85-Ω differential impedance and a 50-Ω, single-ended impedance. A USB pair is routed on a single layer adjacent to a ground plane. USB pairs should not cross plane splits. Limit layer transitions to a minimum. Reference USB pairs to a power plane when necessary. The power plane must be well-bypassed.

2.7 SATA

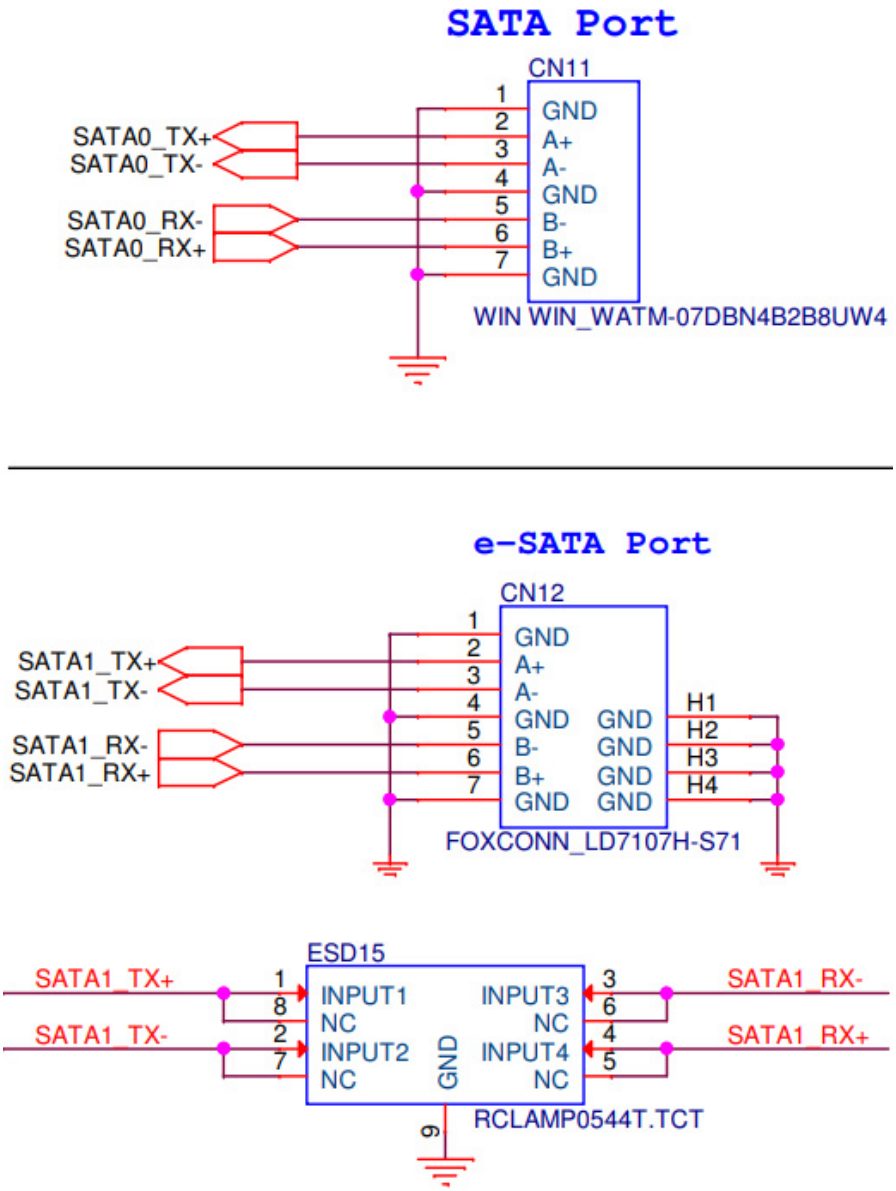
2.7.1 Signal Definitions

Table 8: SATA Signal Description

Signal	Pin	Description	I/O	Remarks
SATA0_RX+ SATA0_RX-	A19 A20	Serial ATA channel 0 Receive input differential pair.	I SATA	
SATA0_TX+ SATA0_TX-	A16 A17	Serial ATA channel 0 Transmit output differential pair.	O SATA	
SATA1_RX+ SATA1_RX-	B19 B20	Serial ATA channel 1 Receive input differential pair.	I SATA	
SATA1_TX+ SATA1_TX-	B16 B17	Serial ATA channel 1 Transmit output differential pair.	O SATA	
SATA2_RX+ SATA2_RX-	A25 A26	Serial ATA channel 2 Receive input differential pair.	I SATA	
SATA2_TX+ SATA2_TX-	A22 A23	Serial ATA channel 2 Transmit output differential pair.	O SATA	
SATA3_RX+ SATA3_RX-	B25 B26	Serial ATA channel 3 Receive input differential pair.	I SATA	
SATA3_TX+ SATA3_TX-	B22 B23	Serial ATA channel 3 Transmit output differential pair.	O SATA	
SATA_ACT#	A28	Serial ATA activity LED. Open collector output pin driven during SATA command activity.	O 3.3V CMOS OC	Able to drive 10 mA

2.7.2 Reference Schematic

Figure 13: SATA Connector Diagram



2.7.3 Routing Considerations

Route SATA signals as differential pairs, with an 85 Ω differential impedance and a 50 Ω, single-ended impedance. Ideally, a SATA pair is routed on a single layer adjacent to a ground plane. SATA pairs should not cross plane splits. Limit layer transitions to a minimum. Carrier Board redrivers on the TX/RX pairs may be necessary.

2.8 LVDS

2.8.1 Signal Definitions

Table 9: LVDS Signal Descriptions

Signal	Pin	Description	I/O
LVDS_A0+ LVDS_A0-	A71 A72	LVDS channel A differential signal pair 0	O LVDS
LVDS_A1+ LVDS_A1-	A73 A74	LVDS channel A differential signal pair 1	O LVDS
LVDS_A2+ LVDS_A2-	A75 A76	LVDS channel A differential signal pair 2	O LVDS
LVDS_A3+ LVDS_A3-	A78 A79	LVDS channel A differential signal pair 3	O LVDS
LVDS_A_CK+ LVDS_A_CK-	A81 A82	LVDS channel A differential clock pair	O LVDS
LVDS_B0+ LVDS_B0-	B71 B72	LVDS channel B differential signal pair 0	O LVDS
LVDS_B1+ LVDS_B1-	B73 B74	LVDS channel B differential signal pair 1	O LVDS
LVDS_B2+ LVDS_B2-	B75 B76	LVDS channel B differential signal pair 2	O LVDS
LVDS_B3+ LVDS_B3-	B77 B78	LVDS channel B differential signal pair 3	O LVDS
LVDS_B_CK+ LVDS_B_CK-	B81 B82	LVDS channel B differential clock pair	O LVDS
LVDS_VDD_EN	A77	LVDS flat panel power enable.	O 3.3V, CMOS
LVDS_BKLT_EN	B79	LVDS flat panel backlight enable high active signal	O 3.3V, CMOS
LVDS_BKLT_CTRL	B83	LVDS flat panel backlight brightness control	O 3.3V, CMOS
LVDS_I2C_CK	A83	DDC I2C clock signal used for flat panel detection and control.	O 3.3V, CMOS
LVDS_I2C_DAT	A84	DDC I2C data signal used for flat panel detection and control.	I/O 3.3V, OD CMOS

2.8.2 Reference Schematics

Figure 14: LVDS Reference Schematic (1)

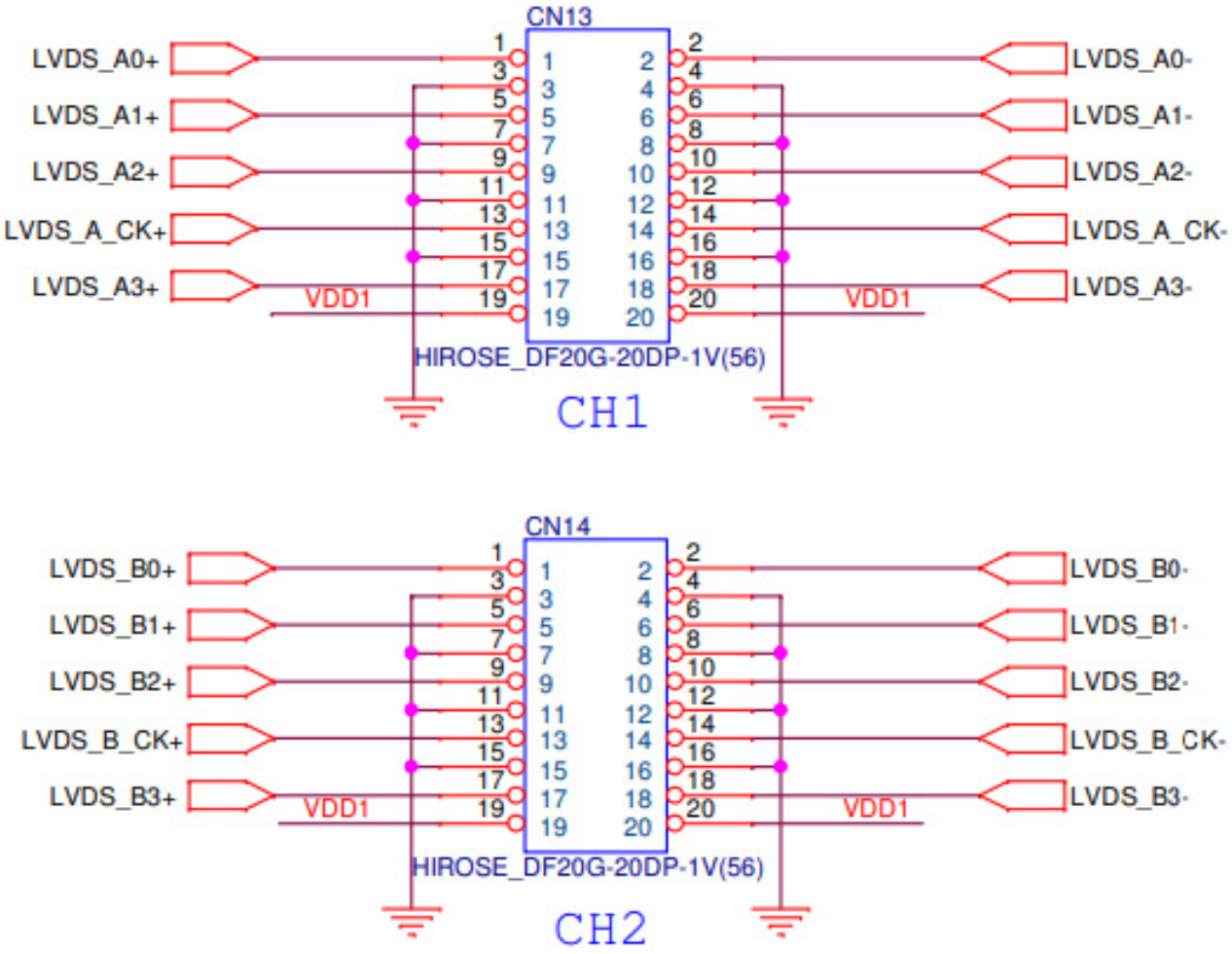
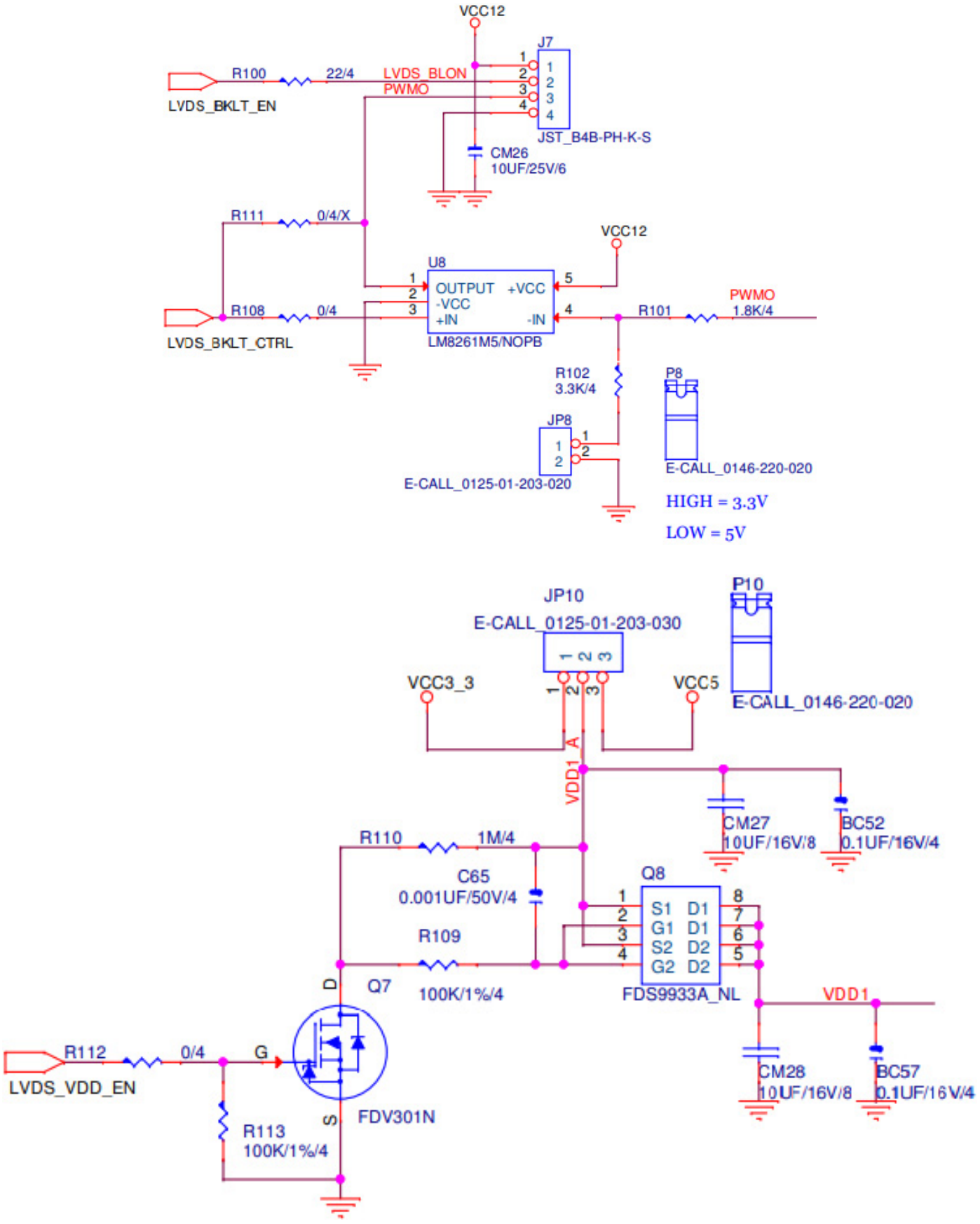


Figure 14: LVDS Reference Schematic (2)



2.8.3 Routing Considerations

Route LVDS signals as differential pairs (excluding the five single-ended support signals), with a 100-Ω differential impedance and a 55-Ω, single-ended impedance. An LVDS pair should be routed on a single layer adjacent to a ground plane. LVDS pairs should not cross plane splits. Keep layer transitions to a minimum. When needed, reference LVDS pairs to a power plane. The power plane must be well-bypassed.

Length-matching between the two lines that make up an LVDS pair (“intra-pair”) and between different LVDS pairs (“inter-pair”) is needed. Intra-pair matching is tighter than the inter-pair matching. All LVDS pairs should have the same environment, including the same reference plane and the same number of vias.

2.9 Embedded DisplayPort (eDP)

2.9.1 Signal Definitions

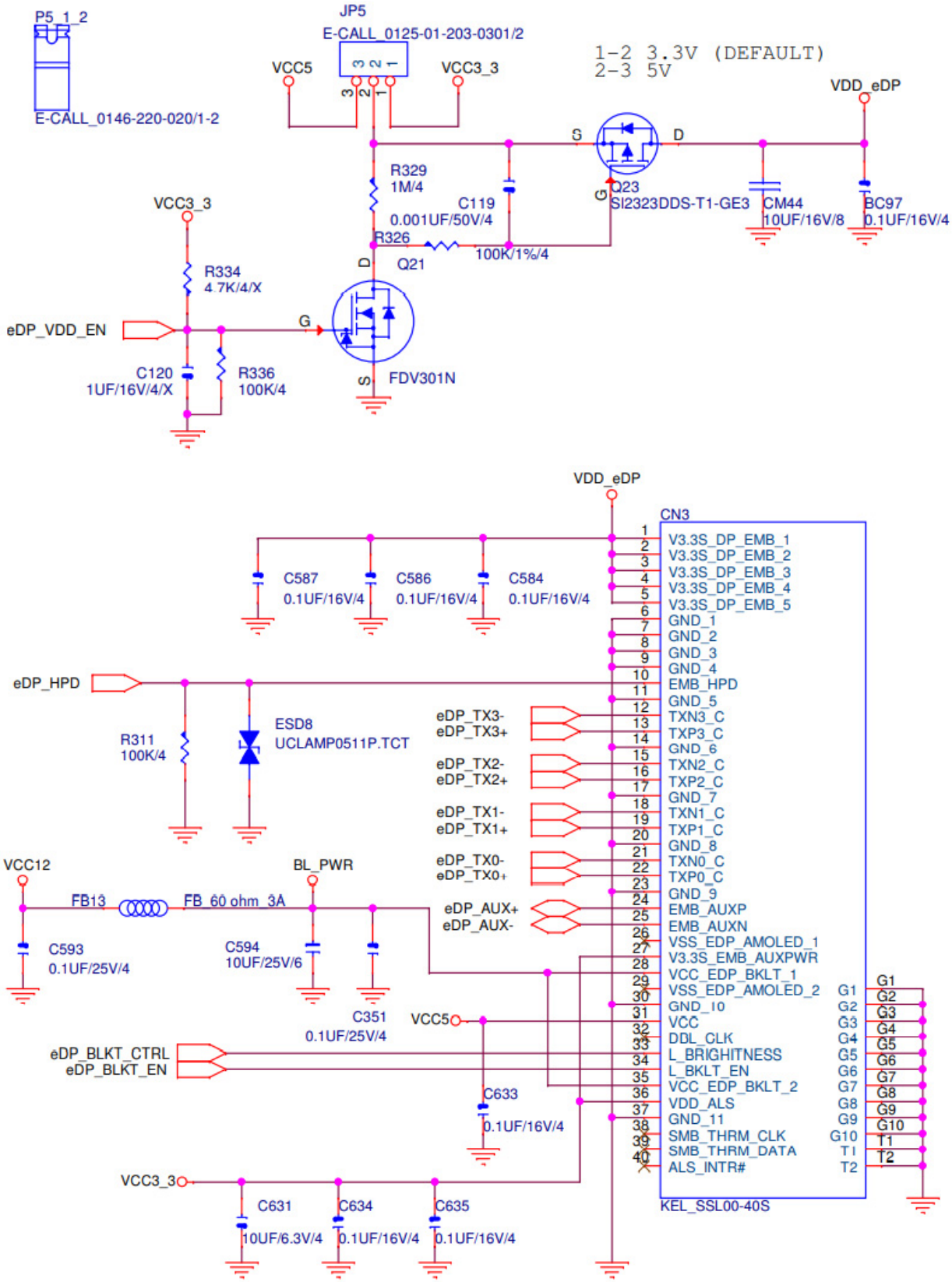
eDP is available in Type 6 and type 10 pin-outs as an alternative to the LVDS A channel. The Module can provide LVDS only, eDP only or Dual-Mode for both interfaces. Refer to the Module documentation for the supported interfaces.

Table 10: eDP Signal Description

Signal	Pins T6/T10	Description	I/O
eDP_TX0+	A75	eDP lane 0, TX +	O PCIe
eDP_TX0-	A76	eDP lane 0, TX -	O PCIe
eDP_TX1+	A73	eDP lane 1, TX +	O PCIe
eDP_TX1-	A74	eDP lane 1, TX -	O PCIe
eDP_TX2+	A71	eDP lane 2, TX +	O PCIe
eDP_TX2-	A72	eDP lane 2, TX -	O PCIe
eDP_TX3+	A81	eDP lane 3, TX +	O PCIe
eDP_TX3-	A82	eDP lane 3, TX -	O PCIe
eDP_VDD_EN	A77	eDP power enable	O CMOS
eDP_BLKT_EN	B79	eDP backlight enable	O CMOS
eDP_BLKT_CTRL	B83	EDP backlight brightness control	O CMOS
eDP_AUX+	A83	eDP auxiliary lane +	I/O PCIe
eDP_AUX-	A84	eDP auxiliary lane -	I/O PCIe
eDP_HPD	A87	Detection of Hot Plug / Unplug and notification of the link layer	I CMOS

2.9.2 Reference Schematics

Figure 15: eDP Reference Schematic



The reference schematic provides a generic eDP interface. The eDP connector used in the design is an example only. Other connectors can be used based on the design requirements. JP5 selects 3.3 or 5V for the panel power. R336 ensures that panel power is disabled when the Module is powering up and before the signal is actively driven. The panel control signals eDP_BLKT_EN, eDP_BLKT_CTRL as well as eDP_HPD are 3.3V level signals. Pay attention to your panel specifications for correct voltage levels and provide translation

2.9.3 Routing Considerations

The traces from JP5 and associated FETs to the eDP connector carry power to the panel. The traces are routed with appropriate thickness to handle the current expected. eDP_TX and eDP_AUX differential pairs are routed as high speed differential pairs. The panel control signals are low speed.

2.10 VGA

2.10.1 Signal Definitions

Table 10: VGA Signal Description

Signal	Pin	HDSUB1	Description	I/O	Remarks
VGA_RED	B89	1	Red component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_GRN	B91	2	Green component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_BLU	B92	3	Blue component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog	Analog output
VGA_HSYNC	B93	13	Horizontal sync output to VGA monitor.	O 3.3V CMOS	
VGA_VSYNC	B94	14	Vertical sync output to VGA monitor.	O 3.3V CMOS	
VGA_I2C_CK	B95	15	DDC clock line (I2C port dedicated to identify VGA monitor capabilities).	O 3.3V CMOS	Level shifter might be necessary
VGA_I2C_DAT	B96	12	DDC data line.	I/O 3.3V CMOS	Level shifter might be necessary
GND		5..8, 10	Analog and Digital GND		
DDC_POWER		9	5V DDC supply voltage for monitor		Power
N.C.		4, 11	Not Connected		

2.10.2 VGA Reference Schematics

Figure 16: VGA Reference Schematics (1)

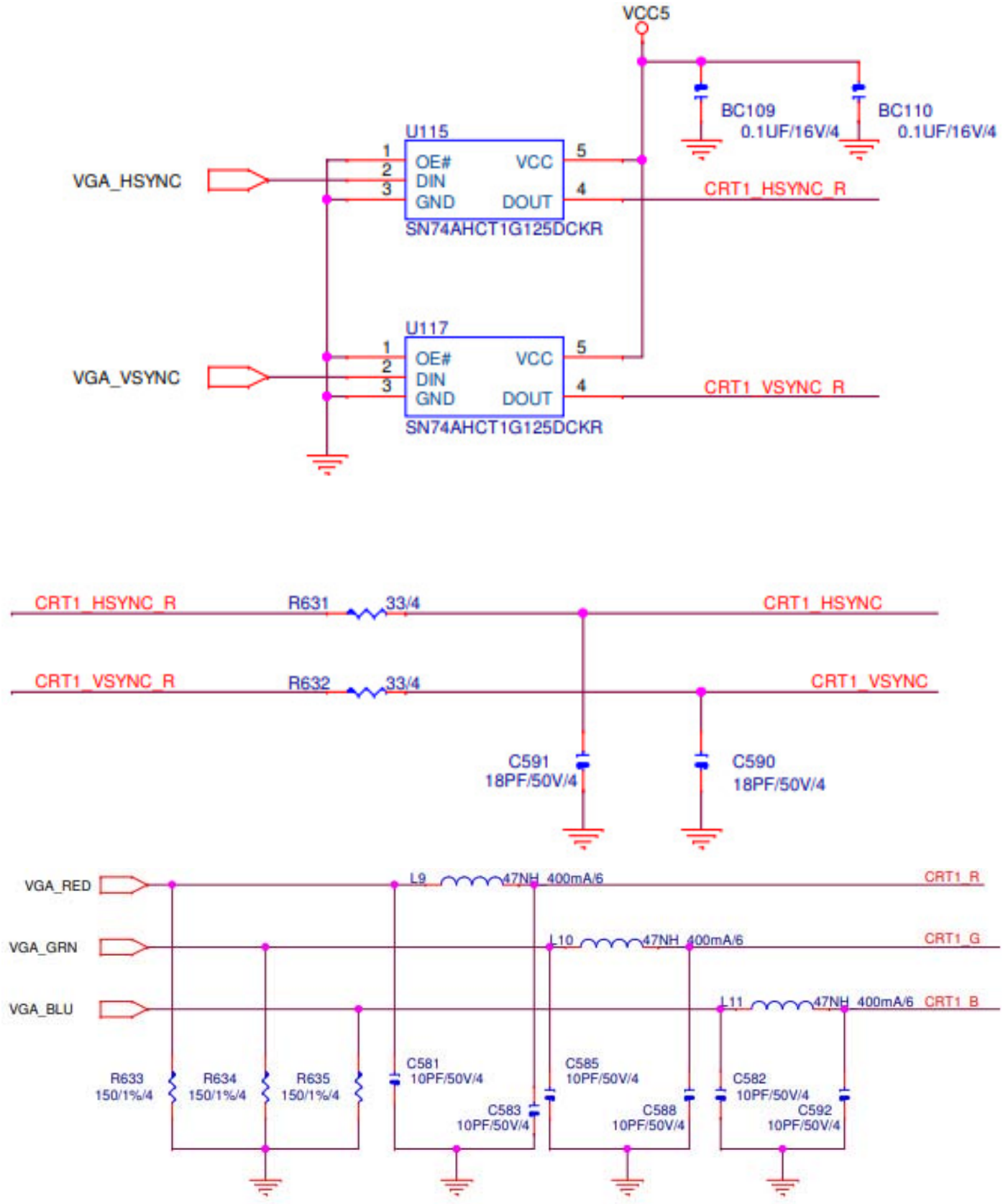
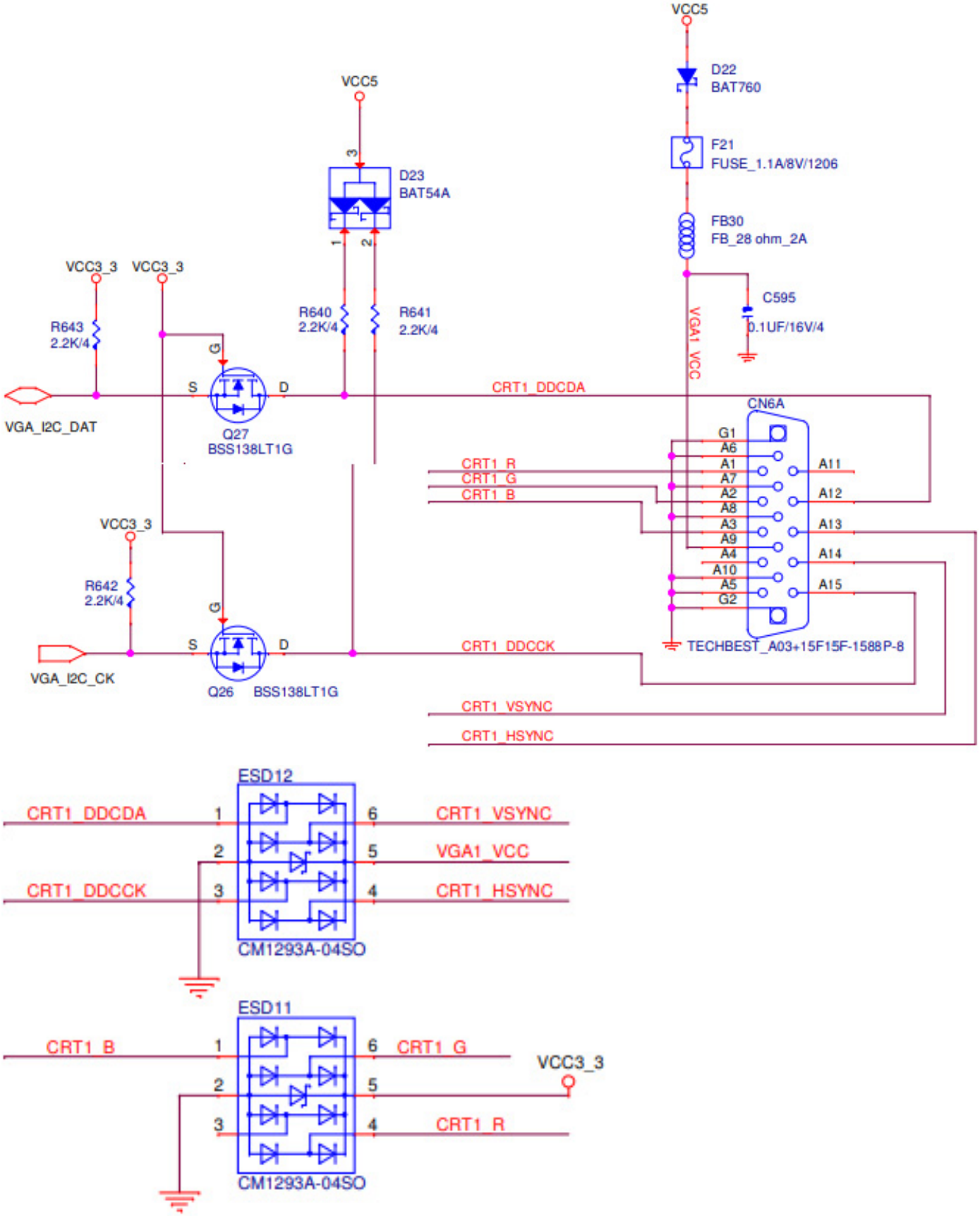


Figure 16: VGA Reference Schematics (2)



2.10.3 Routing Considerations

2.10.3.1 RGB Analog Signals

The RGB signal interface of the COM Express Module has three identical 8-bit digital-to- analog converter (DAC) channels. One each for the red, green, and blue components of the monitor signal. Each channel should have a 150Ω ±1% pull-down resistor connected from the DAC output to the Carrier Board ground. A second 150Ω ±1% termination resistor is available on the COM Express Module itself. An additional 75Ω termination resistor is available within the monitor for each analog DAC output signal. Since the DAC runs at speeds up to 350MHz, pay special attention to signal integrity and EMI. A PI-filter should be placed on each RGB signal that is used to reduce high-frequency noise and EMI. The PI-filter has two 10pF capacitors with a 120Ω @ 100MHz ferrite bead between them. Place the PI-filters and the terminating resistors as close as possible to the standard VGA connector.

2.10.3.2 HSYNC and VSYNC Signals

The horizontal and vertical sync signals 'VGA_HSYNC' and 'VGA_VSYNC' on the COM Express Module are 3.3V tolerant outputs. VGA monitors may drive the monitor sync signals with 5V tolerance, so implement high impedance unidirectional buffers to prevent potential electrical over-stress of the Module and avoid that VGA monitors may attempt to drive the monitor sync signals back to the Module.

To have optimal ESD protection, implement additional low capacitance clamp diodes on the monitor sync signals and placed them between the 5V power plane and ground and close to the VGA connector.

2.10.3.3 DDC Interface

COM Express has a dedicated I2C bus for the VGA interface, corresponding to the VESA defined DDC interface that is used to read out the CRT monitor specific Extended Display Identification Data (EDID). The appropriate signals 'VGA_I2C_DAT' and 'VGA_I2C_CK' of the COM Express Module are supposed to be 3.3V tolerant. Since most VGA monitors drive the internal EDID EEPROM with a supply voltage of 5V, the DDC interface on the VGA connector must also be sourced with 5V. This can be accomplished by placing a 100kΩ pull-up resistors between the 5V power plane and each DDC interface line. Level shifters for the DDC interface signals are required between the COM Express Module signal side and the signals on the standard VGA connector on the Carrier Board.

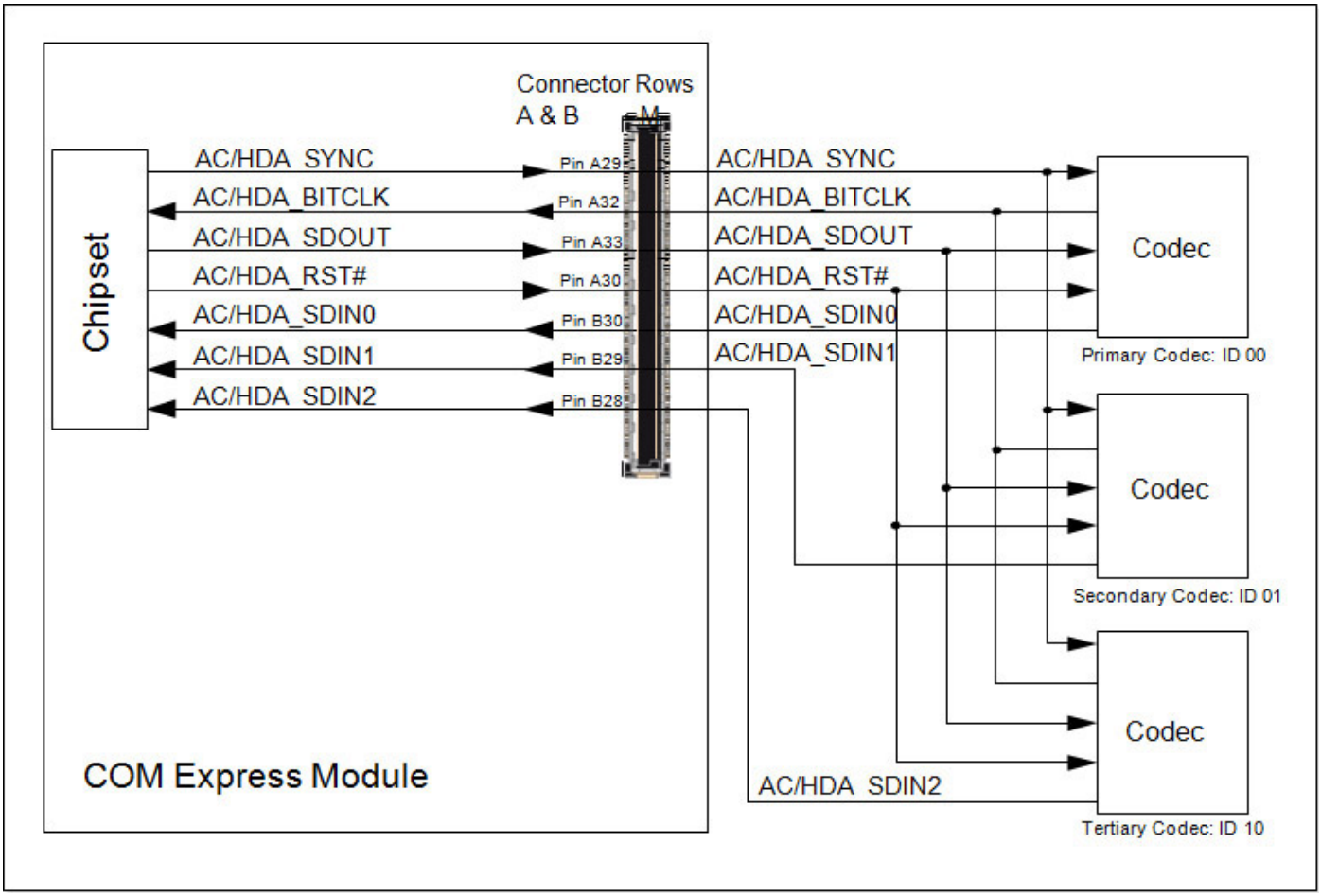
Additional Schottky diodes must be placed between 5V and the pull-up resistors of the DDC signals to avoid backward current leakage during Suspend operation of the Module.

2.11 Digital Audio Interfaces

Table 11: Audio Codec Signal Descriptions

Signal	Pin	Description	I/O
AC/HDA_RST#	A30	CODEC Reset.	O 3.3V Suspend CMOS
AC/HDA_SYNC	A29	Serial Sample Rate Synchronization.	O 3.3V CMOS
AC/HDA_BITCLK	A32	24 MHz Serial Bit Clock for HDA CODEC.	O 3.3V CMOS
AC/HDA_SDOUT	A33	Audio Serial Data Output Stream.	O 3.3V CMOS
AC/HDA_SDIN0 AC/HDA_SDIN1 AC/HDA_SDIN2	B30 B29 B28	Audio Serial Data Input Stream from CODEC[0:2].	I 3.3V Suspend CMOS

Figure 17: Multiple Audio Codec Configuration



2.11.1 Reference Schematics

2.11.1.1 High Definition Audio

Figure 18: HDA Example Schematic (1)

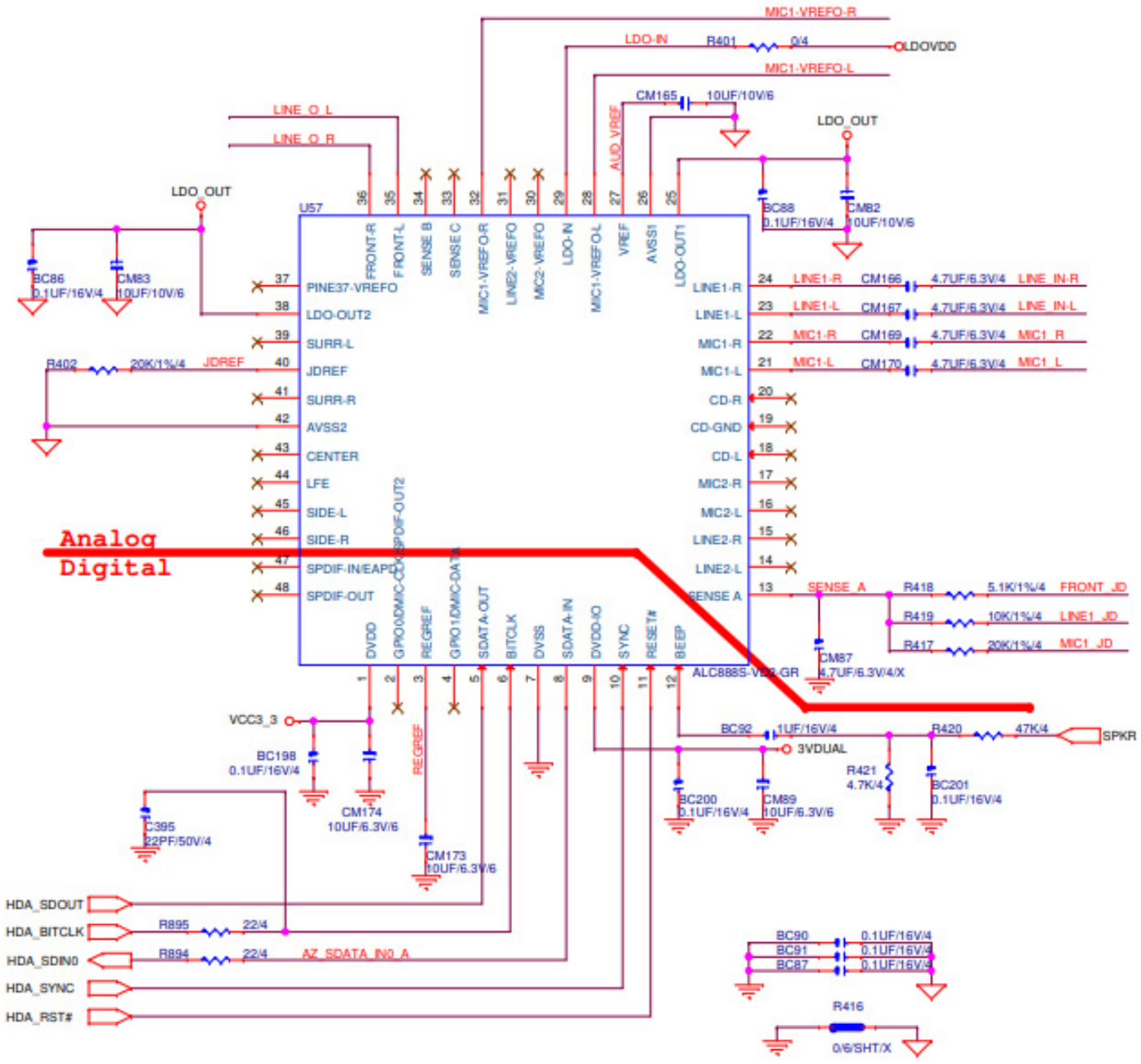
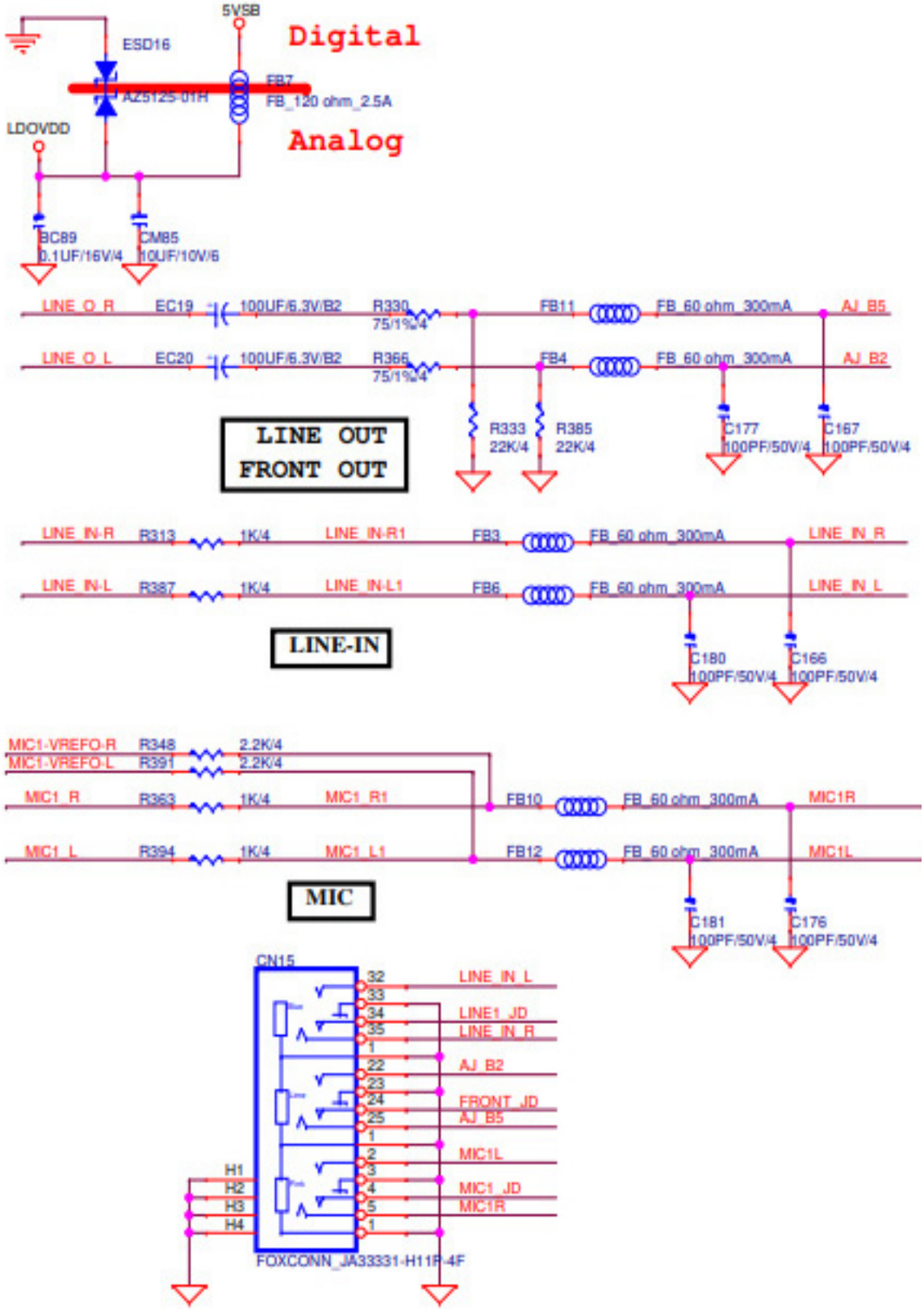


Figure 18: HDA Example Schematic (2)



2.11.2 Routing Considerations

Route traces with a target impedance of 55Ω with a tolerance of ±15%. Pay attention to ground return paths for the analog signals. Digital signals routed in the vicinity of the analog audio signals should not cross the power plane split lines. The analog and digital signals are to be far from each other. Partition the Carrier Board with all analog components grouped together in one area and group all digital components in another area.

Keep digital signal traces far from the analog input and voltage reference pins. Give separate analog and digital ground planes with the digital components over the digital ground plane, and the analog components, like analog power regulators, over the analog ground plane. The split between the planes must be at least 0.05 inch wide.

Route analog power and signal traces over the analog ground plane. Route digital power and signal traces over the digital ground plane. Place bypassing and decoupling capacitors close to the IC pins with wide traces to minimize impedance. Place the crystal or oscillator near the codec.

Do not fully isolate the analog/audio ground plane from the rest of the Carrier Board ground plane. Give a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between the planes must be at least 0.05 inch wide.

Signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main Carrier Board ground. No signal should cross the split/gap between the ground planes to prevent a ground loop that will increase EMI emissions and degrade the signal quality.

2.12 LPC Bus – Low Pin Count Interface

2.12.1 Signal Definition

Table 12: LPC Interface Signal Descriptions

Signal	Pin	Description	I/O	Comment
LPC_SERIRQ	A50	LPC serialized IRQ.	I/O 3.3V CMOS	
LPC_FRAME#	B3	LPC frame indicates start of a new cycle or termination of a broken cycle.	O 3.3V CMOS	
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3	B4 B5 B6 B7	LPC multiplexed command, address and data.	I/O 3.3V CMOS	
LPC_DRQ0# LPC_DRQ1#	B8 B9	LPC encoded DMA/Bus master request.	I 3.3V CMOS	Not all Modules support LPC DMA. Contact your vendor for information.
LPC_CLK	B10	LPC clock output 33MHz.	O 3.3V CMOS	

2.12.2 LPC Bus Reference Schematics

2.12.2.1 Super I/O

Figure 19: LPC Super I/O Example (1)

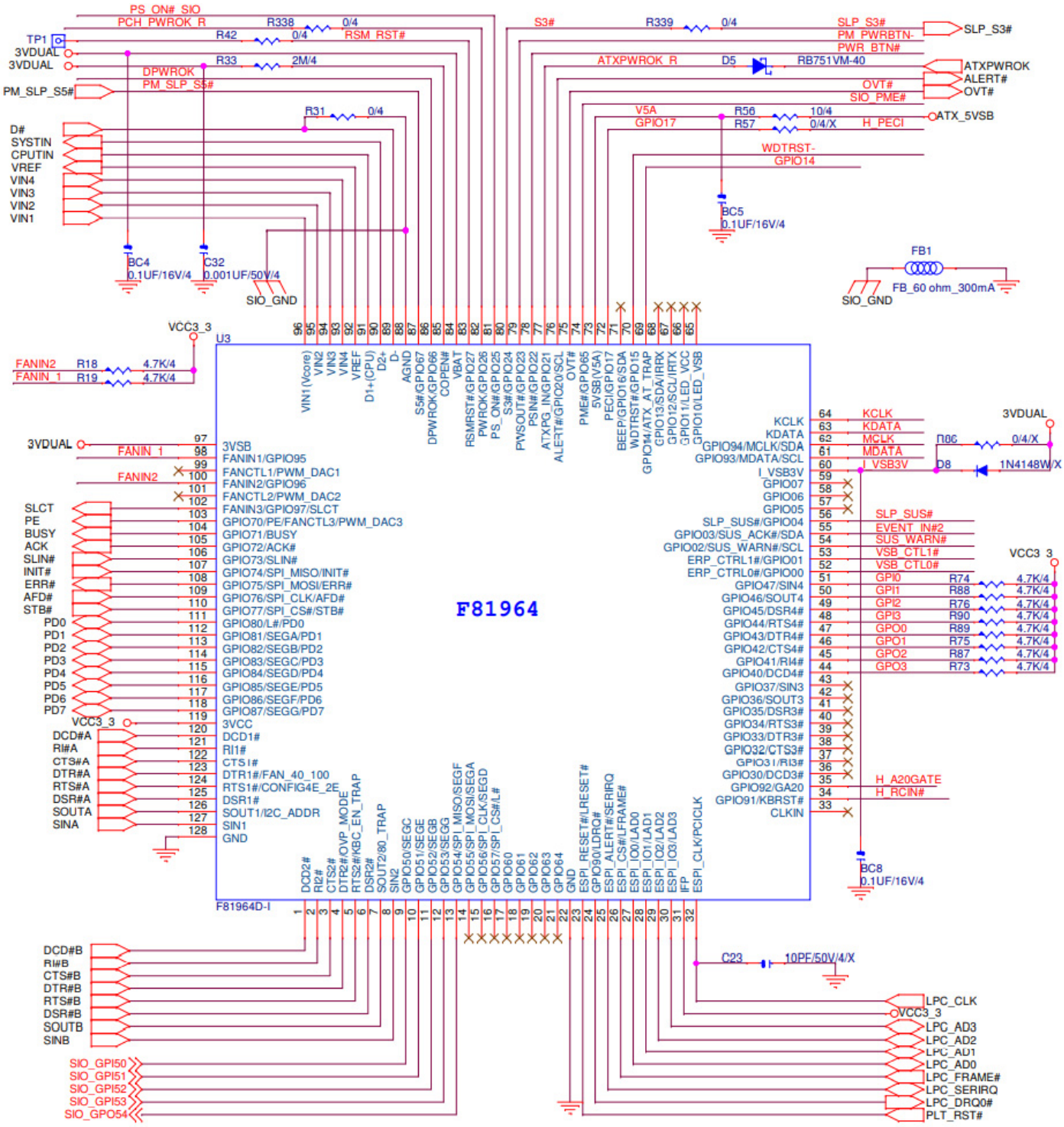


Figure 19: LPC Super I/O Example (2)

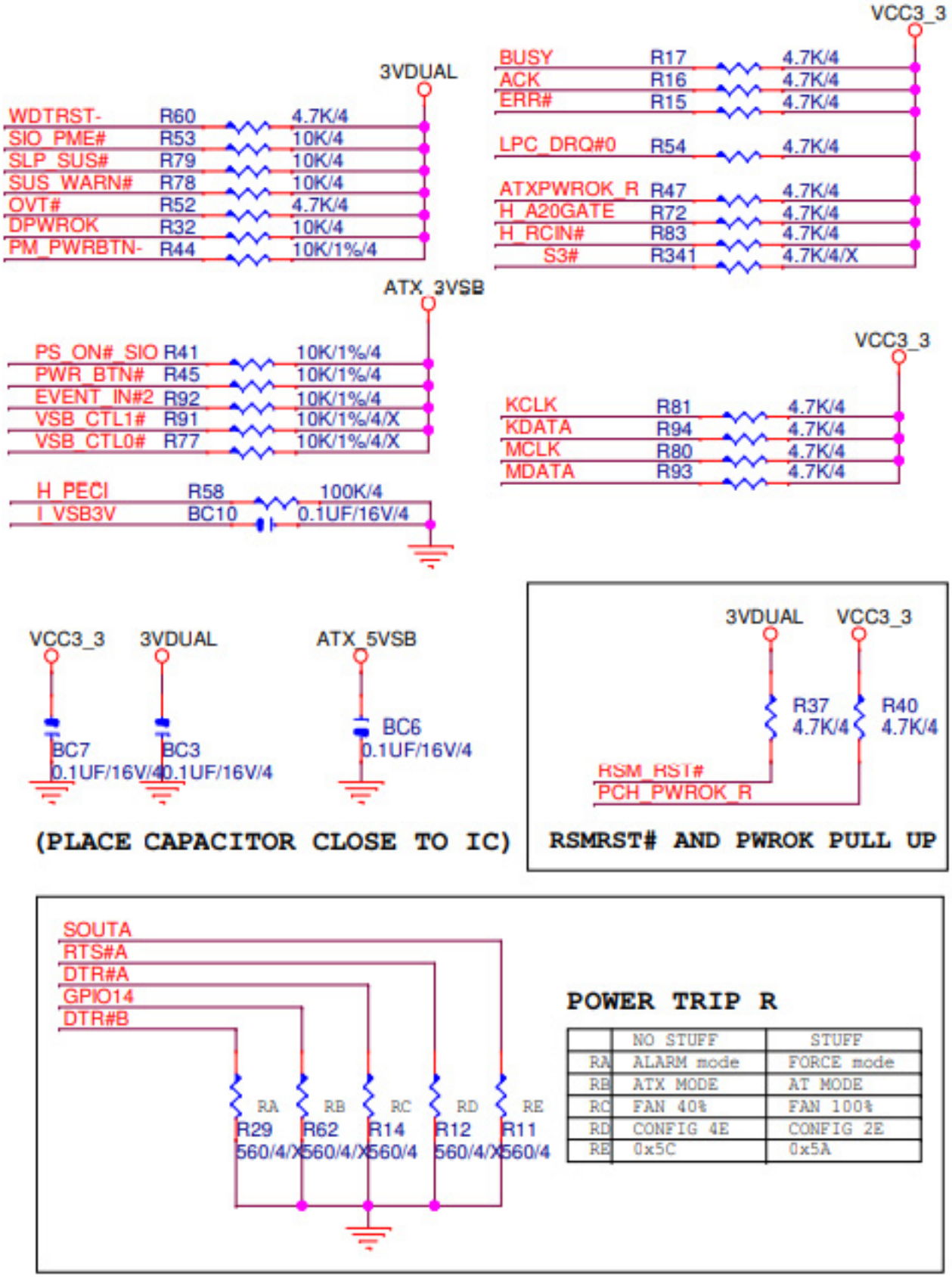


Figure 20: LPC Firmware Hub

Please refer to:
PICMG COM Express Carrier Board Design Guide
Rev. 2.0 / December 6, 2013
Page 207 Figure 80 LPC Firmware Hub

2.12.3 Routing Considerations

2.12.3.1 General Signals

LPC signals are similar to PCI signals. Route the LPC bus as 55 Ω, single-ended signals. The bus preferably should be referenced to ground, or to a well-bypassed power plane or a combination of the two. Point-to-point (daisy-chain) routing is recommended. Stubs up to 1.5 inches are acceptable. Length-matching among LPC_AD[3:0], LPC_FRAME# are necessary.

Please refer to:
PICMG COM Express Carrier Board Design Guide
Rev. 2.0 / December 6, 2013
Section 6.6.3 'LPC Trace Routing Guidelines' on page 193.

2.13 Serial Peripheral Interface Bus

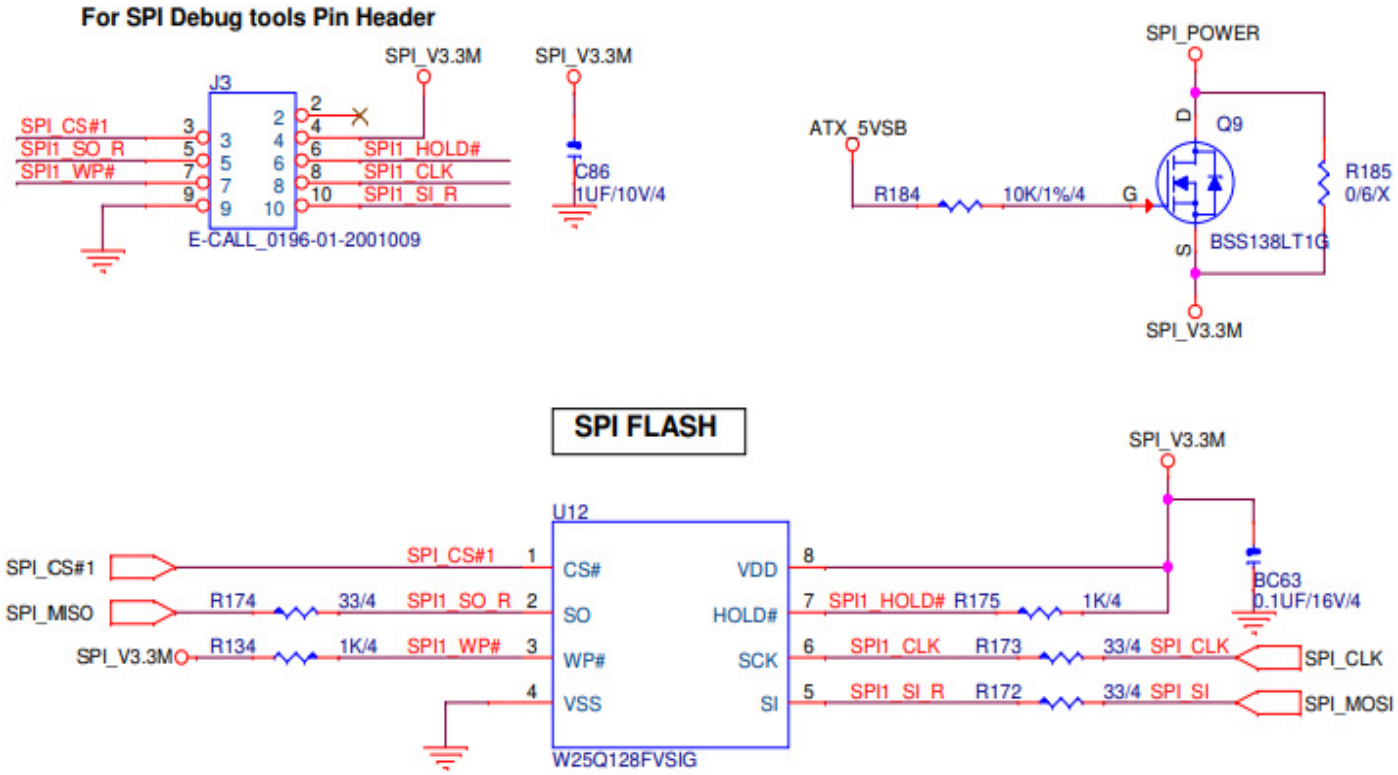
2.13.1 Signal Definition

Table 13: SPI Signal Definition

Signal	Pin	Description	I/O
SPI_CS#	B97	Chip select for Carrier Board SPI – may be sourced from chipset SPI0 or SPI1	O CMOS – 3.3V Suspend
SPI_MISO	A92	Data in to Module from Carrier SPI	I CMOS – 3.3V Suspend
SPI_MOSI	A95	Data out from Module to Carrier SPI	O CMOS – 3.3V Suspend
SPI_CLK	A94	Clock from Module to Carrier SPI	O CMOS – 3.3V Suspend
SPI_POWER	A91	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier.	O – 3.3V Suspend
BIOS_DIS0#	A34	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to for strapping options of BIOS disable signals.	I CMOS
BIOS_DIS1#	B88	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, Effect of the BIOS disable signals on page 119 IPICMG COM Express Carrier Board Design Guide, Rev. 20 / December 6, 2013) for strapping options of BIOS disable signals.	I CMOS

2.13.2 SPI Reference Schematics

Figure 21: SPI Reference Schematics



2.13.3 Routing Considerations

The SPI signals SPI_MISO, SPI_MOSI, SPI_CS# and SPI_CLK should be routed with a maximum length of 4.5” and should match to each other within 0.1”.

2.14 General Purpose I2C Bus Interface

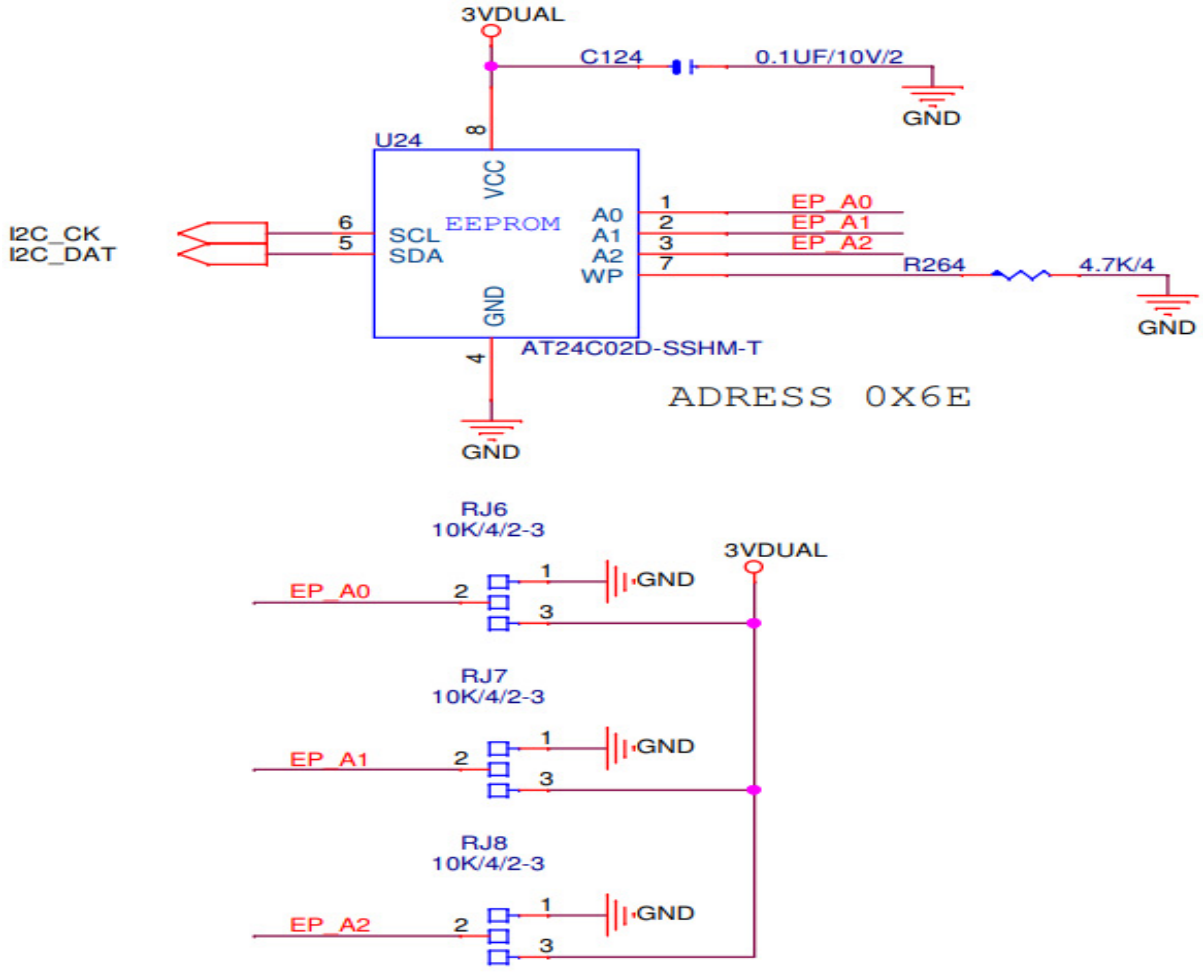
2.14.1 Signal Definitions

Table 14: General Purpose I2C Interface Signal Descriptions

Signal	Pin	Description	I/O	Power Rail
I2C_CK	B33	General Purpose I2C Clock output	I/O OD CMOS	3.3V Suspend
I2C_DAT	B34	General Purpose I2C data I/O line.	I/O OD CMOS	3.3V Suspend

2.14.2 Reference Schematics

Figure 22: System Configuration EEPROM Circuitry

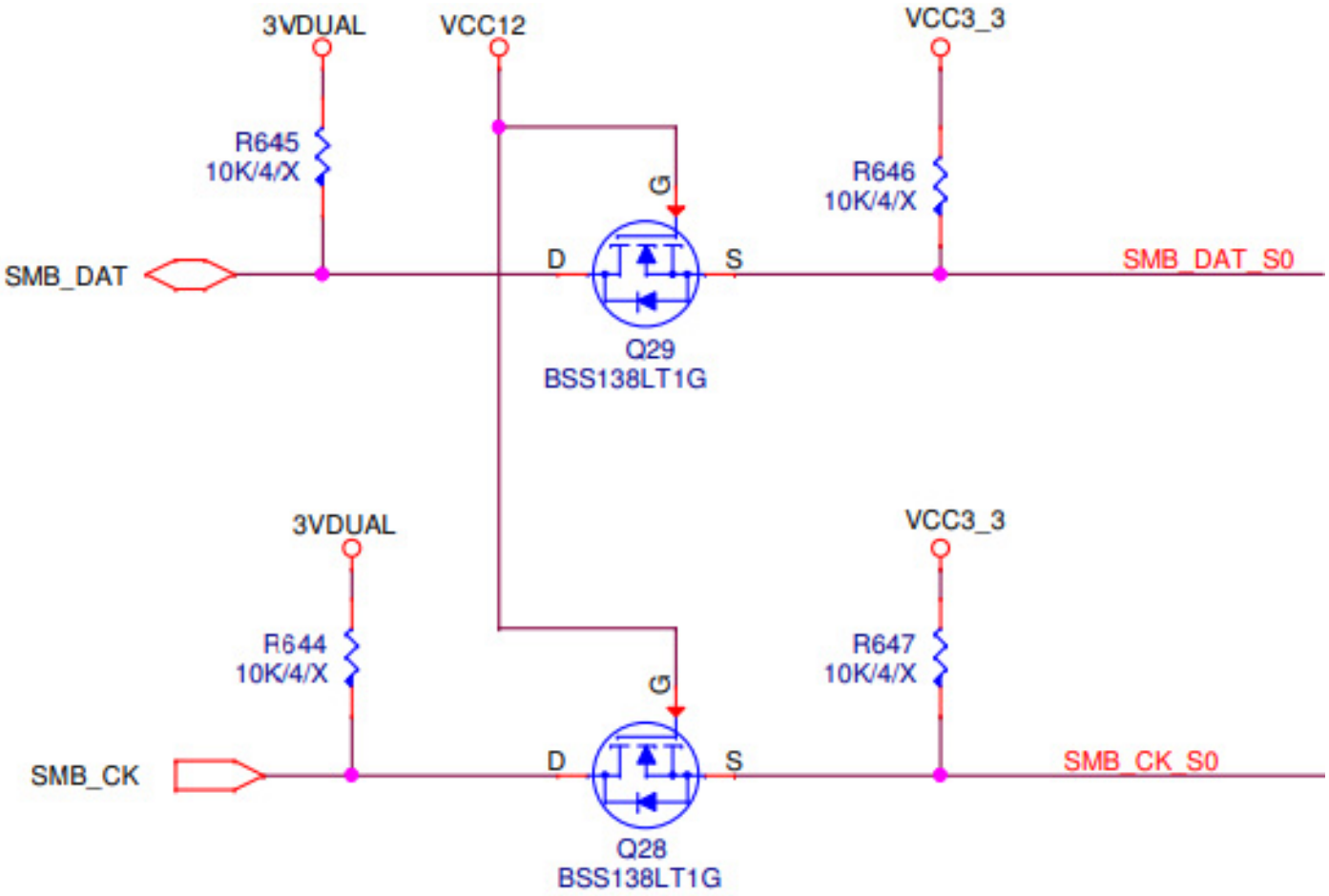


2.14.3 Connectivity Considerations

The maximum capacitance allowed on the Carrier General Purpose I2C bus lines (I2C_DAT, I2C_CK) is specified by the module vendor. The carrier designer should ensure that the maximum capacitance is not exceeded and the rise/fall times of the signals meet the I2C bus specification. As a rule, an IC input has 8pF of capacitance, and a PCB trace has 3.8pF per inch of trace length.

2.15 System Management Bus (SMBus)

Figure 23: System Management Bus Separation



2.15.1 Signal Definitions

Table 15: System Management Bus Signals

Signal	Pin	Description	I/O	Power Rail
SMB_CK	B13	System Management Bus bidirectional clock line	I/O OD CMOS	3.3V Suspend rail
SMB_DAT	B14	System Management bidirectional data line.	I/O OD CMOS	3.3V Suspend rail
SMB_ALERT#	B15	System Management Bus Alert	I CMOS	3.3V Suspend Rail

2.15.2 Routing Considerations

The SMBus should be connected to all or none of the PCIe/PCI devices and slots. Do not connect these devices to the SMBus. The maximum load of SMBus lines is limited to 3 external devices.

Do not connect Non-Suspend powered devices to the SMBus unless a bus switch is used to prevent back feeding of voltage from the Suspend rail to other supplies.

2.16 General Purpose Serial Interface

2.16.1 Signal Definitions

Table 16: General Purpose Serial Interface Signal Definition

Signal	Pin	Description	I/O
SER0_TX	A98	Transmit Line for Serial Port 0	O CMOS (protected)
SER0_RX	A99	Receive Line for Serial Port 0	I CMOS (protected)
SER1_TX	A101	Transmit Line for Serial Port 1 (can be shared with CAN function)	O CMOS (protected)
SER1_RX	A102	Receive Line for Serial Port 1 (can be shared with CAN function)	I CMOS (protected)

2.16.2 Reference Schematics

2.16.2.1 General Purpose Serial Port Example

Figure 24: General Purpose Serial Port Example (1)

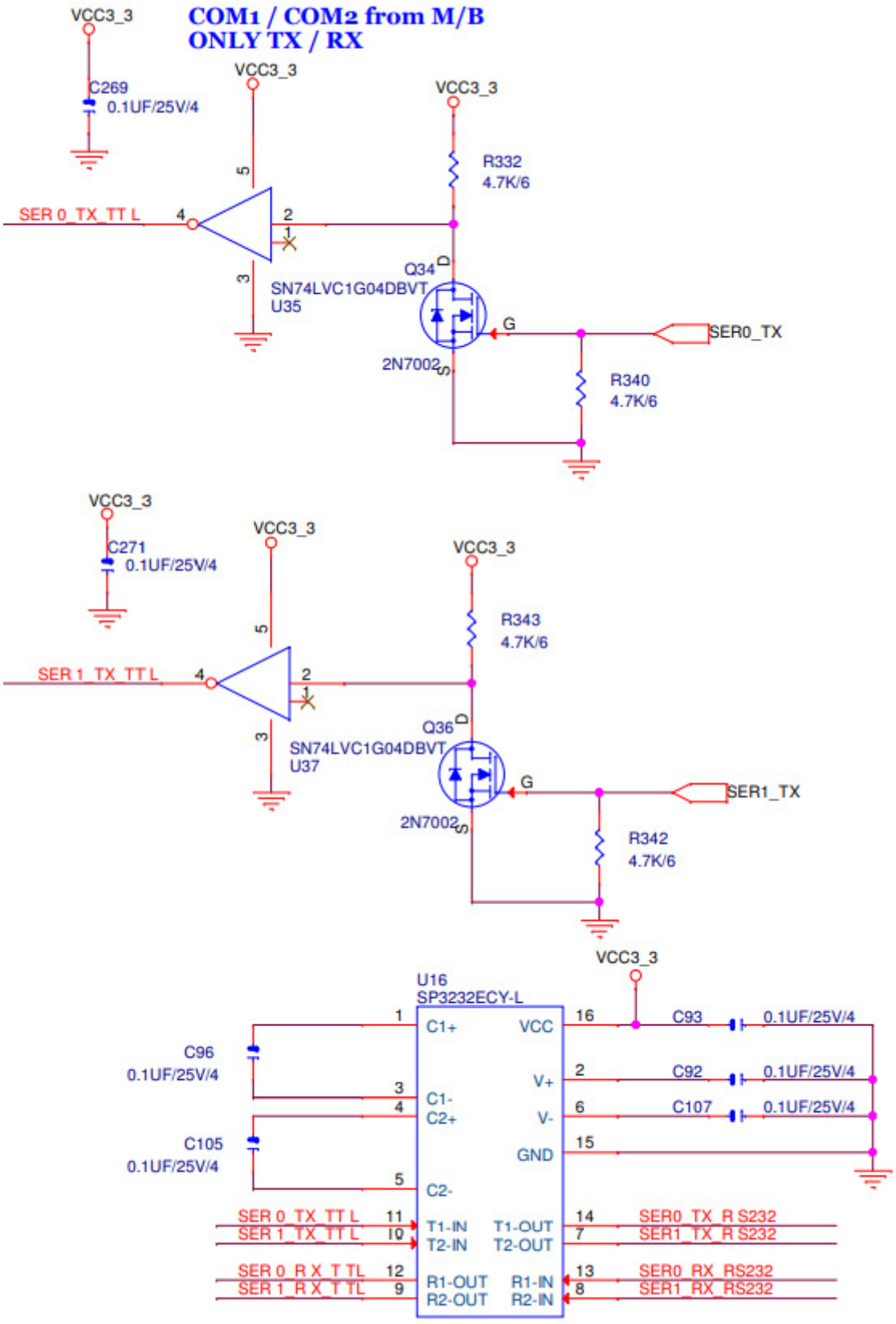
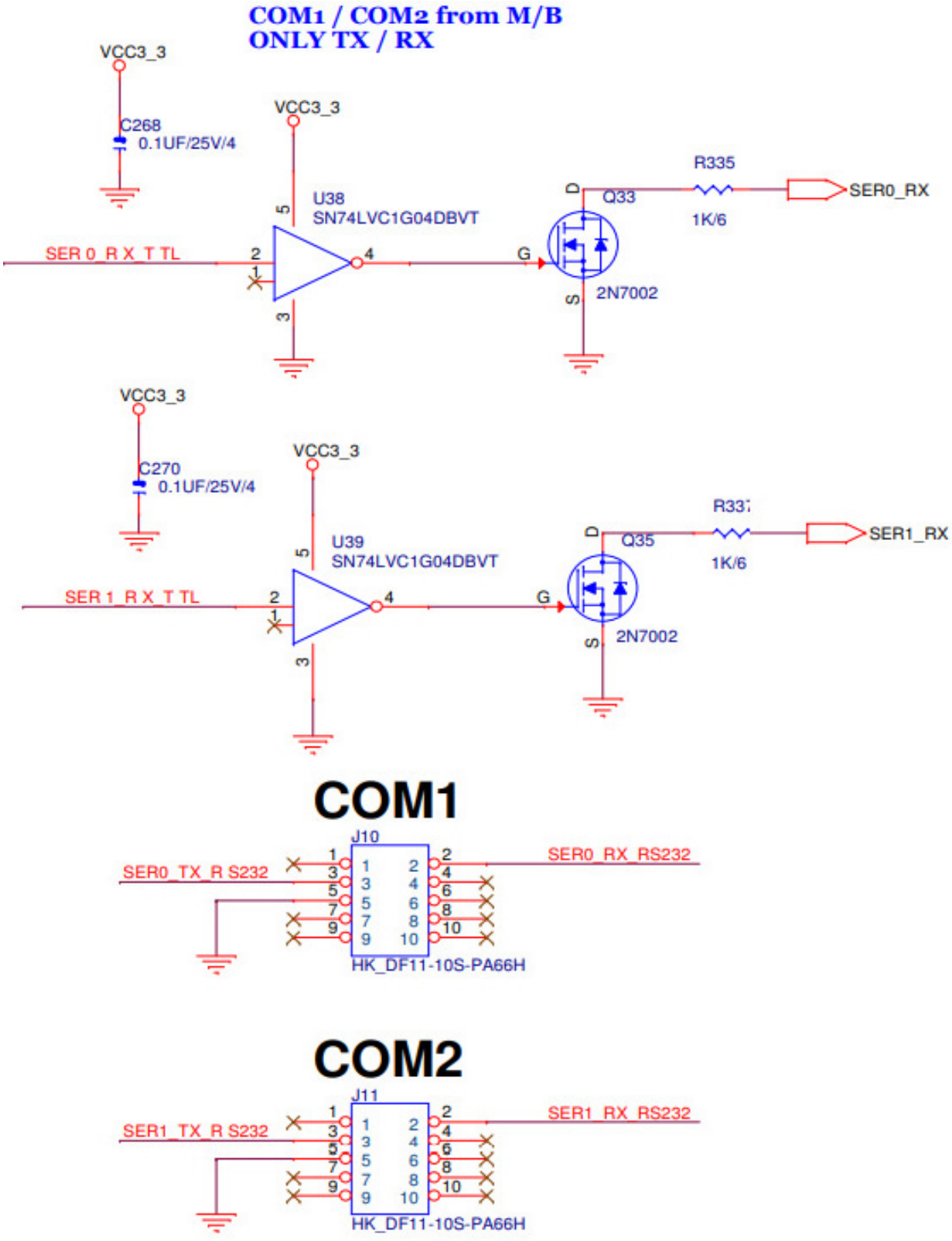


Figure 24: General Purpose Serial Port Example (2)



2.16.3 Routing Considerations

There are no further routing considerations that need to be taken.

2.17 CAN Interface

2.17.1 Signal Definitions

Table 17: CAN Interface Signal Definition

Signal	Pin	Description	I/O
CAN_TX	A101	Transmit Line for CAN (can be shared with SER1 function)	O CMOS (protected)
CAN_RX	A102	Receive Line for CAN (can be shared with SER1 function)	I CMOS (protected)

2.17.2 Reference Schematics

Figure 25: CAN Bus Example (1)

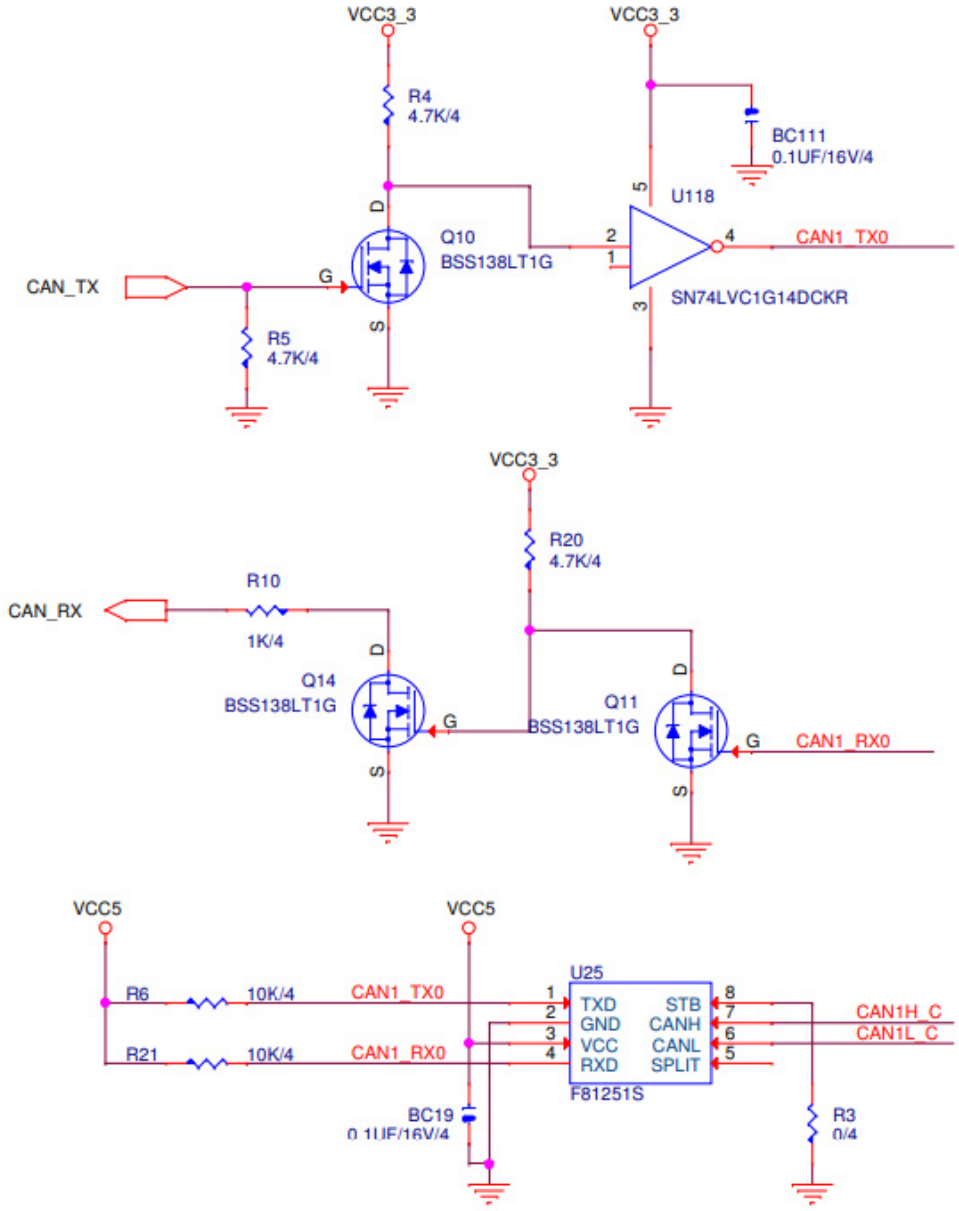
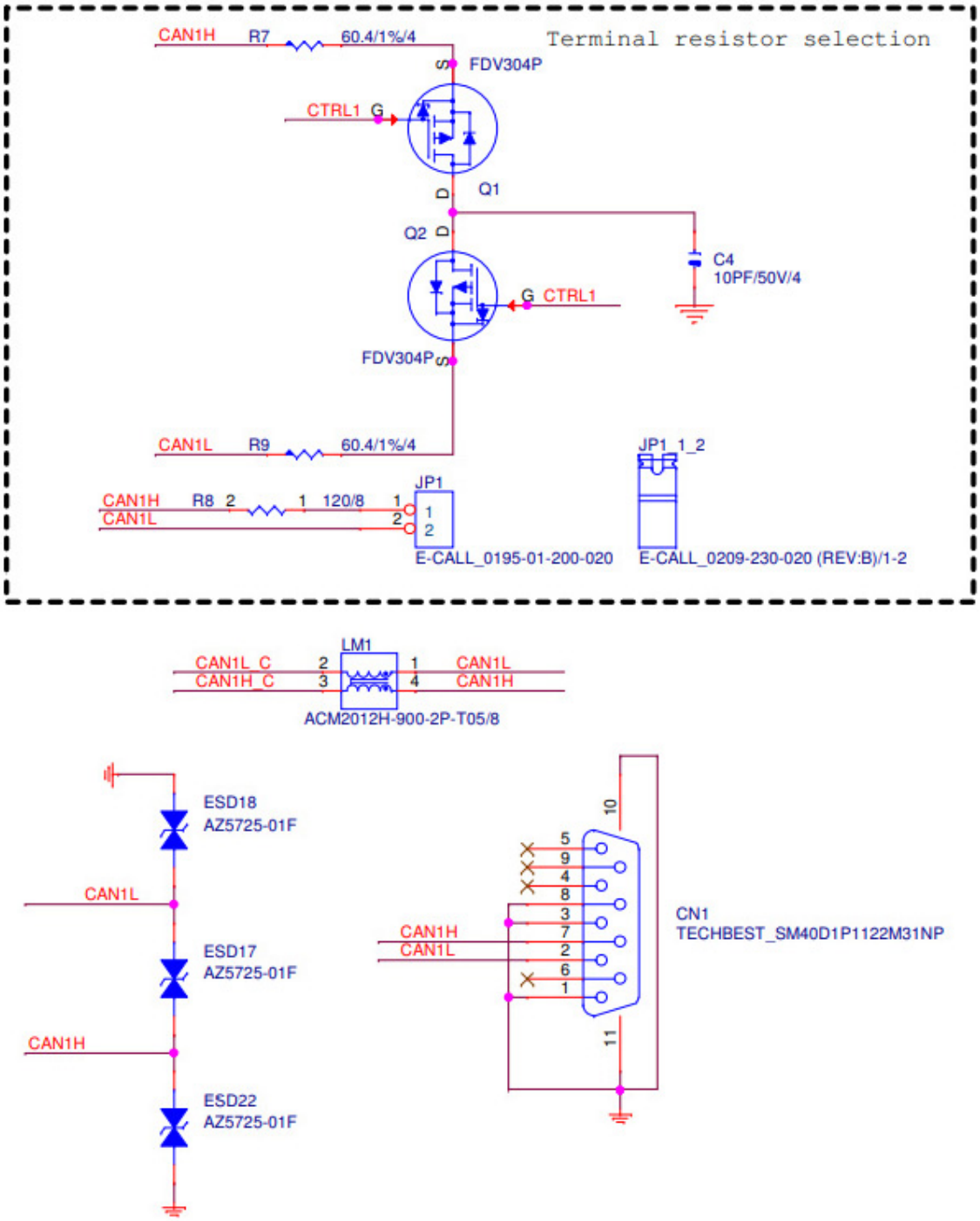


Figure 25: CAN Bus Example (2)



2.17.3 Routing Considerations

It should be routed as a differential pair signal with 120 Ohm differential impedance. The end points of CAN bus should be terminated with 120 Ohms or with 60 Ohms from the CAN_H line and 60 Ohms from the CAN_L line to the CAN Bus reference voltage. Check your CAN transceiver application notes on termination.

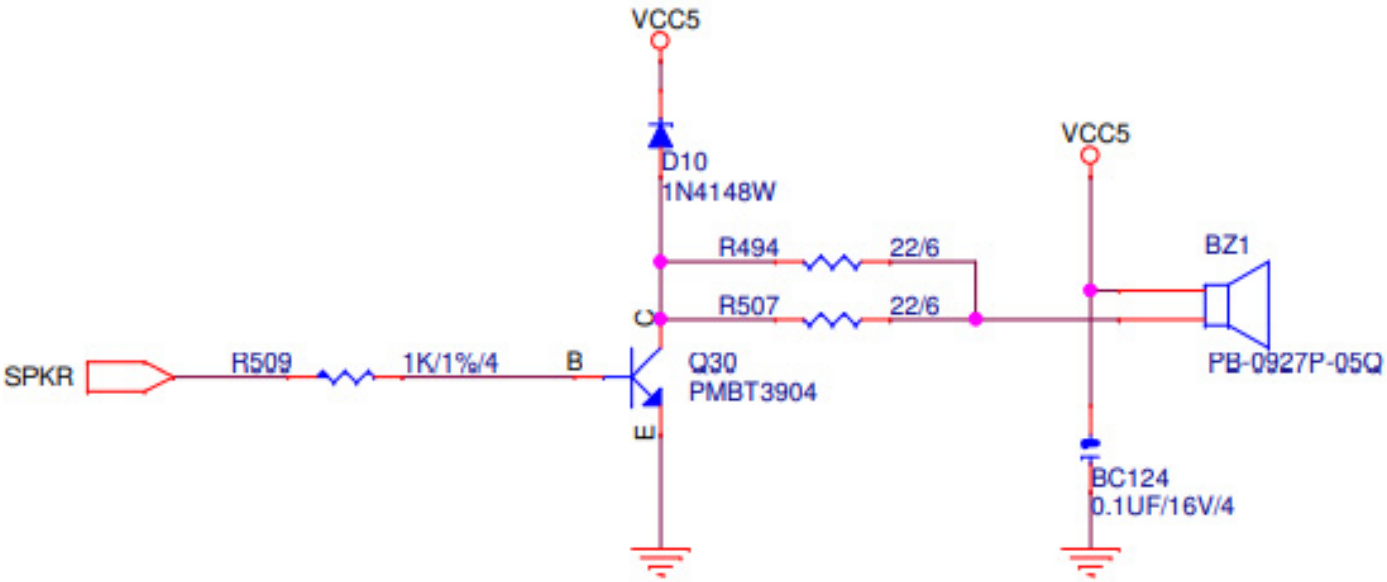
2.18 Miscellaneous Signals

Table 18: Miscellaneous Signals

Signal	Pin	Description	I/O	Remarks
TYPE0# TYPE1# TYPE2#	C54 C57 D57	The Type pins indicate the COM Express pin-out type of the Module. To indicate the Module's pin-out type, the pins are either not connected or strapped to ground on the Module. The Carrier Board has to implement additional logic, which prevents the system to switch power on, if a Module with an incompatible pin-out type is detected.	O 5V PDS	Only Available on T2-T6
TYPE10#	A97	Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier Board, that a Rev 1.0/2.0 Module is installed. TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47k 12V Pin-out R1.0		
SPKR	B32	Output used to control an external FET or a logic gate to drive an external PC speaker.	O 3.3V CMOS	
BIOS_DISABLE0#	A34	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low,	I 3.3V CMOS	**Refer to SPI – Serial Peripheral**
BIOS_DISABLE1#	B88	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low,	I 3.3V CMOS	**Refer to SPI – Serial Peripheral**
WDT	B27	Output indicating that a watchdog time-out event has occurred.	O 3.3V CMOS	
KBD_RST#	A86	Input signal of the Module used by an external keyboard controller to force a system reset.	I 3.3V CMOS	Only Available on T1-T5
KBD_A20GATE	A87	Input signal of the Module used by an external keyboard controller to control the CPU A20 gate line. The A20 gate restricts the memory access to the bottom megabyte of the system. Pulled high on the Module.	I 3.3V CMOS	Only Available on T1-T5
LID#	A103	LID switch. Low active signal used by the ACPI operating system for a LID switch.	I 3.3V CMOS OD	Only Available on T6 and T10
SLEEP#	B103	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3V CMOS OD	Only Available on T6 and T10
FAN_PWMOUT[1]	B101	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 3.3V CMOS OD	Only Available on T6 and T10
FAN_TACHIN[1]	B102	Fan tachometer input for a fan with a two pulse output.	I 3.3V CMOS OD	Only Available on T6 and T10
TPM_PP[1]	A96	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V CMOS	Only Available on T6 and T10
GPO0 GPO1 GPO2 GPO3	A93 B54 B57 B63	General Purpose Outputs for system specific usage.	O 3.3V CMOS	Refer to the Module's users guide for information of the
GPI0 GPI1 GPI2 GPI3	A54 A63 A67 A85	General Purpose Input for system specific usage. The signals are pulled up by the Module.	I 3.3V CMOS	Refer to the Module's users guide for information of the

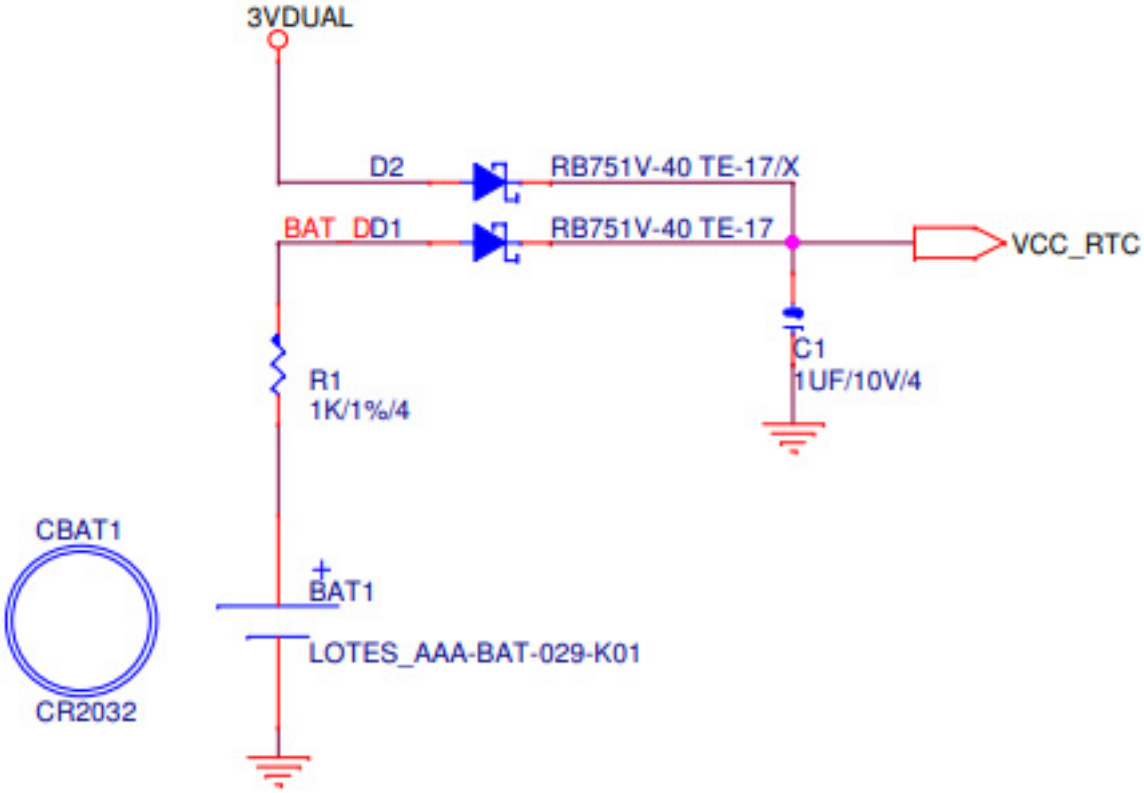
2.18.1 Speaker Output

Figure 26: Speaker Output Circuitry



2.18.2 RTC Battery Implementation

Figure 27: RTC Battery Circuitry with Serial Schottky Diode



2.18.3 Power Management Signals

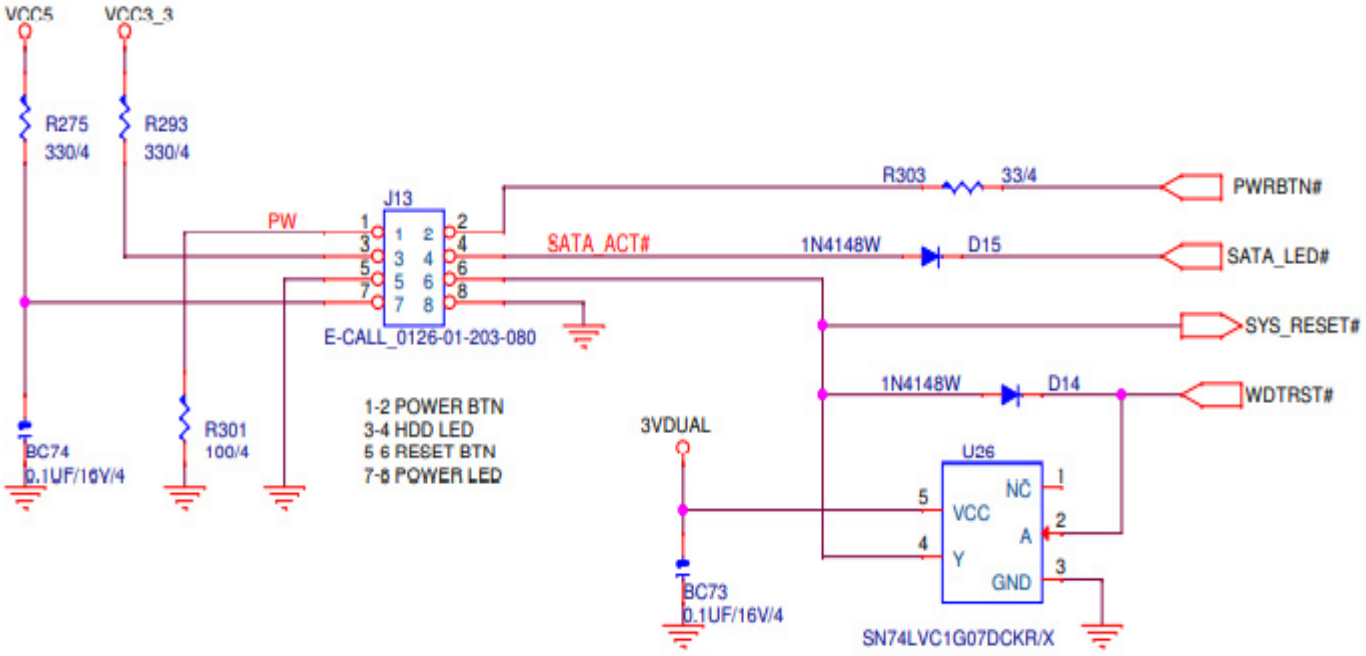
Table 19: System States S0-S5 Definitions

System State	Description	Power Rail State
S0 Full On	All components are powered and the system is fully functional.	Full power on all power rails.
S1 Power-on Standby (POS)	In sleeping state, no system context is lost, hardware maintains all system context. During S1 operation some system components are set into low power state.	Full power on all power rails.
S2	Not supported.	
S3 Suspend to RAM (STR)	The current system state and context is stored in main memory and all unnecessary system logic is turned off.	Only main memory and logic required to wake-up the system remain powered by the Suspend voltages. All other power rails are switched off.
S4 Suspend to Disk (STD) Hibernate	The current system state and context is stored on disk and all unnecessary system logic is turned off. S4 is similar to S5 and just supported by OS.	Similar to S5; All other power rails are switched off.
S5 Soft Off	In S5 state the system is switched off. Restart is only possible with the power button or by a system wake-up event such as 'Wake On LAN' or RTC alarm.	Suspend power rails are powered. All other power rails are switched off.

Table 20: Power Management Signal Descriptions

Signal	Pin	Description	I/O	Remarks
PWRBTN#	B12	Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge.	I 3.3V Suspend CMOS	Drive with >=10mA
SYS_RESET#	B49	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3V Suspend CMOS	Drive with >=10mA
CB_RESET#	B50	Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board.	O 3.3V Suspend CMOS	
PWR_OK	B24	Power OK status signal generated by the ATX power supply to notify the Module that the DC operating voltages are within the ranges required for proper operation.	I 3.3V CMOS	
SUS_STAT#	B18	Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode.	O 3.3V Suspe nd CMOS	
SUS_S3#	A15	S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM).	O 3.3V Suspend CMOS	This signal can be used to control the ATX power supply via the *'PS_ON#'* signal.
SUS_S4#	A18	S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk).	O 3.3V Suspend CMOS	
SUS_S5#	A24	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off).	O 3.3V Suspend CMOS	
WAKE0#	B66	PCI Express wake-up event signal.	I 3.3V Suspend CMOS	
WAKE1#	B67	General purpose wake-up signal.	I 3.3V Suspend CMOS	
BATLOW#	A27	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used	I 3.3V Suspend CMOS	

Figure 28: PWRBTN# and SYS_RESET# Circuitry



2.18.4 Watchdog Timer

Figure 29: Watchdog Timer Event Latch Schematic

Please refer to:
PICMG COM Express Carrier Board Design Guide
Rev. 2.0 / December 6, 2013
Page 137 Figure 54: Watchdog Timer Event Latch Schematic

2.18.5 General Purpose Input/Output (GPIO)

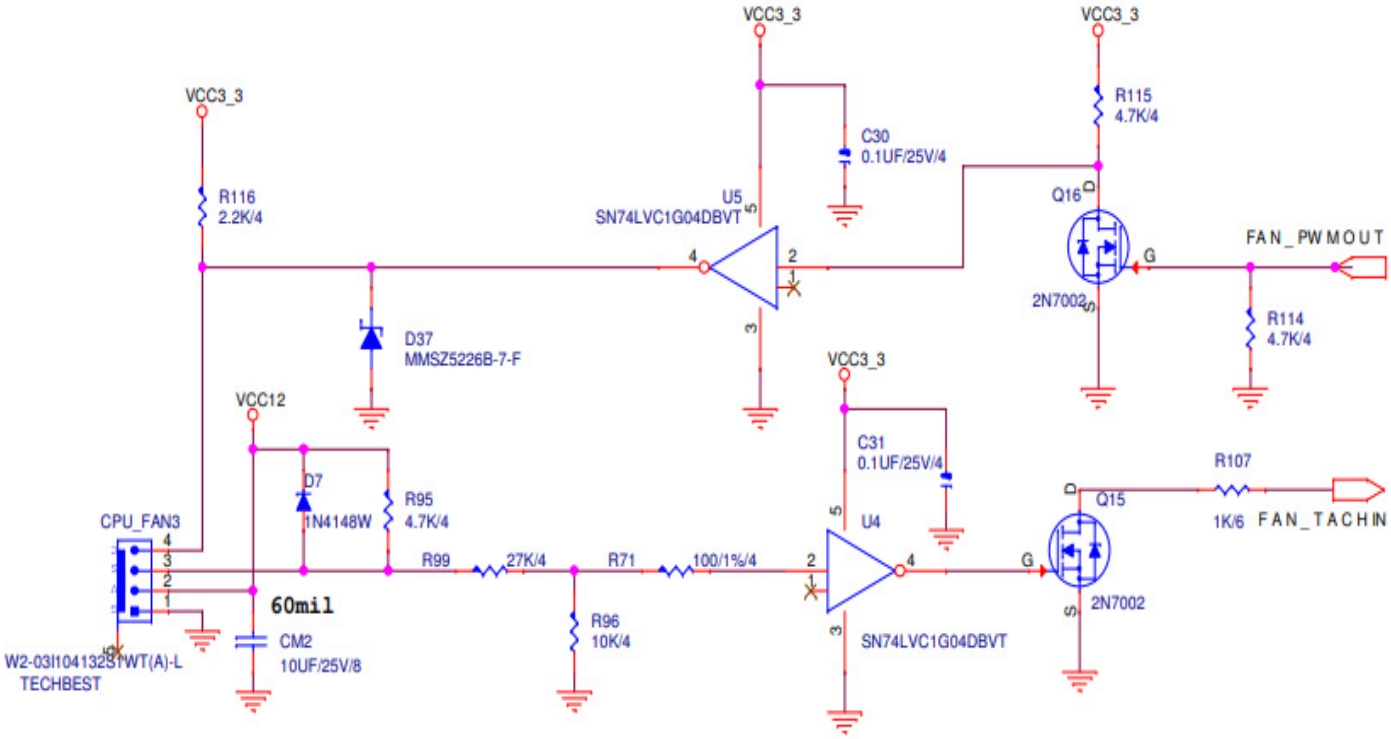
Table 21: GPIO Signal Definition

Signal	Pin	Description	I/O
GPI0	A54	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS
GPI1	A63	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS
GPI2	A67	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS
GPI3	A85	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS
GPO0	A93	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS
GPO1	B54	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS
GPO2	B57	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS
GPO3	B63	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS

Figure 30: General Purpose I/O Loop-back Schematic
Please refer to:
PICMG COM Express Carrier Board Design Guide
Rev. 2.0 / December 6, 2013
Page 139 Figure 55: General Purpose I/O Loop-back Schematic

2.18.6 Fan Connector

Figure 31: Fan Connector Reference Schematic



2.18.7 Thermal Interface

Table 22: Thermal Management Signal Descriptions

Signal	Pin	Description	I/O
THRM#	B35	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	I 3.3V CMOS
THRMTRIP#	A35	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	O 3.3V CMOS

2.19 PCI Bus

2.19.1 Signal Definitions

Table 23: PCI Bus Signal Definition

Signal	Pin#	Description	I/O	Remarks
PCI_AD0	C24	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD1	D22	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD2	C25	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD3	D23	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD4	C26	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD5	D24	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD6	C27	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD7	D25	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD8	C28	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD9	D27	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD10	C29	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD11	D28	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD12	C30	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD13	D29	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD14	C32	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD15	D30	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD16	D37	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD17	C39	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD18	D38	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD19	C40	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD20	D39	PCI bus multiplexed address and data lines	I/O 3.3V	IDSEL for slot 0
PCI_AD21	C42	PCI bus multiplexed address and data lines	I/O 3.3V	IDSEL for slot 1
PCI_AD22	D40	PCI bus multiplexed address and data lines	I/O 3.3V	IDSEL for slot 2
PCI_AD23	C43	PCI bus multiplexed address and data lines	I/O 3.3V	IDSEL for slot 3
PCI_AD24	D42	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD25	C45	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD26	D42	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD27	C46	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD28	D44	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD29	C47	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD30	D45	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_AD31	C48	PCI bus multiplexed address and data lines	I/O 3.3V	
PCI_C/BE0#	D26	PCI bus byte enable line 0, active low	I/O 3.3V	
PCI_C/BE1#	C33	PCI bus byte enable line 0, active low	I/O 3.3V	
PCI_C/BE2#	C38	PCI bus byte enable line 0, active low	I/O 3.3V	
PCI_C/BE3#	C44	PCI bus byte enable line 0, active low	I/O 3.3V	
PCI_DEVSEL#	C36	PCI bus Device Select, active low	I/O 3.3V	
PCI_Frame#	D36	PCI bus Frame control line, active low	I/O 3.3V	
PCI_IRDY#	C37	PCI bus Initiator Ready control line, active low	I/O 3.3V	
PCI_TRDY#	D35	PCI bus Target Ready control line, active low	I/O 3.3V	

Signal	Pin#	Description	I/O	Remarks
PCI_STOP#	D34	PCI bus STOP control line, active low	I/O 3.3V	
PCI_PAR	D32	PCI bus parity	I/O 3.3V	
PCI_PERR#	C34	Parity Error: An external PCI device drivers PERR# by driving it low, when it receives data that has a parity error.	I/O 3.3V	
PCI_REQ0#	C22	PCI bus master request input line, active low	I 3.3V	
PCI_REQ1#	C19	PCI bus master request input line, active low	I 3.3V	
PCI_REQ2#	C17	PCI bus master request input line, active low	I 3.3V	
PCI_REQ3#	D20	PCI bus master request input line, active low	I 3.3V	
PCI_GNT0#	C20	PCI bus master grant output line, active low	O 3.3V	
PCI_GNT1#	C18	PCI bus master grant output line, active low	O 3.3V	
PCI_GNT2#	C16	PCI bus master grant output line, active low	O 3.3V	
PCI_GNT3#	D19	PCI bus master grant output line, active low	O 3.3V	
PCI_RESET#	C23	PCI Reset output, active low	O 3.3V_SBY	Asserted during system reset
PCI_LOCK#	C35	PCI Lock control line, active low	I/O 3.3V	
PCI_SERR#	D33	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition	I/O 3.3V	
PCI_PME#	C15	PCI Power Management Event: PCI peripherals drive PME# to low to wake up the system from low-power states S1-S5	I 3V3_SBY	
PCI_CLKRUN#	D48	Bidirectional pin used to support PCI clock run protocol for mobile systems.	I/O 3.3V	
PCI_IRQA#	C49	PCI interrupt request line A	I 3.3V	
PCI_IRQB#	C50	PCI interrupt request line B	I 3.3V	
PCI_IRQC#	D46	PCI interrupt request line C	I 3.3V	
PCI_IRQD#	D47	PCI interrupt request line D	I 3.3V	
PCI_CLK	D50	PCI 33MHz clock output	O 3.3V	
PCI_M66EN	D49	Module input signal that indicates whether a Carrier Board PCI device is capable of 66MHz operation. It is pulled to ground by Carrier Board device or by slot card, if one of the devices is NOT capable of 66MHz operation.	I 3.3V	

2.19.2 Reference Schematics

2.19.2.1 Resource Allocation

Figure 32: PCI Bus Interrupt Routing

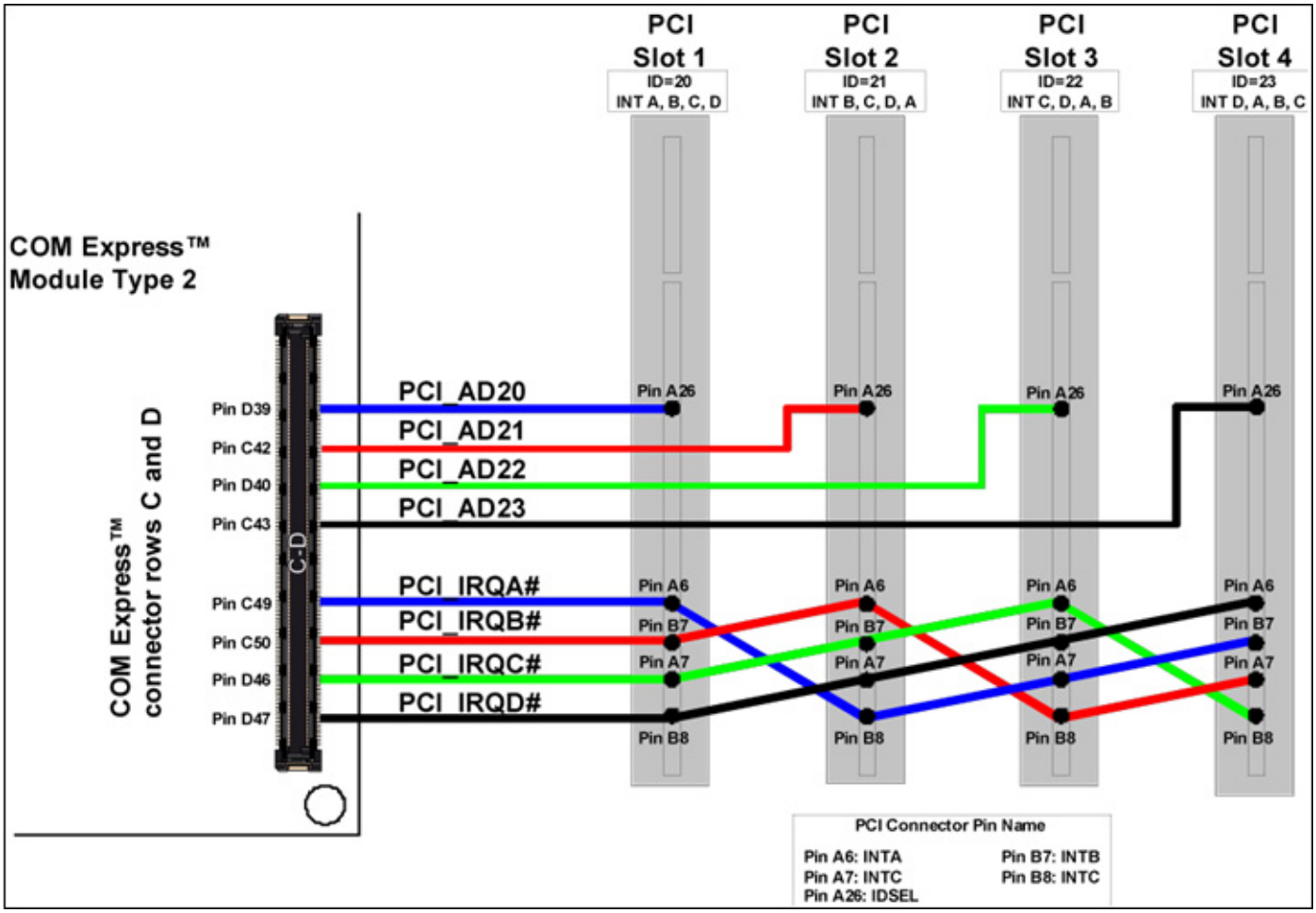


Table 24: PCI Bus Interrupt Routing

Device Signal	Slot / Device 1	Slot / Device 2	Slot / Device 3	Slot / Device 4
IDSEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB# (if used)	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC# (if used)	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTC# (if used)	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#

2.19.3.1 Device-Down Example

Figure 33: PCI Device Down Example; Dual UART

Please refer to:
PICMG COM Express Carrier Board Design Guide
Rev. 2.0 / December 6, 2013
Page 150 Figure 60: PCI Device Down Example; Dual UART

2.20 IDE and CompactFlash (PATA)

2.20.1 Signal Definitions

Table 25: Parallel ATA Signal Descriptions

Signal	Pin	Description	I/O	IDE40	IDE44	CF
IDE_D0	D7	Bidirectional data to / from IDE device.	I/O 3.3V	17	17	21
IDE_D1	C10	Bidirectional data to / from IDE device.	I/O 3.3V	15	15	22
IDE_D2	C8	Bidirectional data to / from IDE device.	I/O 3.3V	13	13	23
IDE_D3	C4	Bidirectional data to / from IDE device.	I/O 3.3V	11	11	2
IDE_D4	D6	Bidirectional data to / from IDE device.	I/O 3.3V	9	9	3
IDE_D5	D2	Bidirectional data to / from IDE device.	I/O 3.3V	7	7	4
IDE_D6	C3	Bidirectional data to / from IDE device.	I/O 3.3V	5	5	5
IDE_D7	C2	Bidirectional data to / from IDE device.	I/O 3.3V	3	3	6
IDE_D8	C6	Bidirectional data to / from IDE device.	I/O 3.3V	4	4	47
IDE_D9	C7	Bidirectional data to / from IDE device.	I/O 3.3V	6	6	48
IDE_D10	D3	Bidirectional data to / from IDE device.	I/O 3.3V	8	8	49
IDE_D11	D4	Bidirectional data to / from IDE device.	I/O 3.3V	10	10	27
IDE_D12	D5	Bidirectional data to / from IDE device.	I/O 3.3V	12	12	28
IDE_D13	C9	Bidirectional data to / from IDE device.	I/O 3.3V	14	14	29
IDE_D14	C12	Bidirectional data to / from IDE device.	I/O 3.3V	16	16	30
IDE_D15	C5	Bidirectional data to / from IDE device.	I/O 3.3V	18	18	31
IDE_A[0:2]	D13-D15	Address lines to IDE device.	O 3.3V	35, 33, 36	35, 33, 36	20, 19, 18
IDE_IOW#	D9	I/O write line to IDE device.	O 3.3V	23	23	35
IDE_IOR#	C14	I/O read line to IDE device.	O 3.3V	25	25	34
IDE_REQ	D8	IDE device DMA request. It is asserted by	I 3.3V	21	21	37
IDE_ACK#	D10	IDE device DMA acknowledge.	O 3.3V	29	29	44
IDE_CS1#	D16	IDE device chip select for 1F0h to 1FFh	O 3.3V	37	37	7
IDE_CS3#	D17	IDE device chip select for 3F0h to 3FFh	O 3.3V	38	38	32
IDE_IORDY	C13	IDE device I/O ready input. Pulled low by	I 3.3V	27	27	42
IDE_RESET#	D18	Reset output to IDE device, active low.	O 3.3V	1	1	41
IDE_IRQ	D12	Interrupt request from IDE device.	I 3.3V	31	31	43
IDE_CBLID#	D77	Input from off-Module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 modes.	I 3.3V	34	34	46
DASP				39	39	45
GND				2, 19, 22, 24, 26, 30, 40	2, 19, 22, 24, 26, 30, 40, 43	17, 16, 15, 14, 12, 11, 10, 8, 12, 6, 9, 33, 25, 26 39 (master)
CSEL				28	28	39
N.C.				20, 32	20, 32, 44	24, 40, 51, 52, 53, 54, 55, 56 39 (slave)
VCC_5V					41, 42,	13, 18, 36

Figure 34: IDE 40 Pin and CompactFlash 50 Pin Connector

Please refer to:
PICMG COM Express Carrier Board Design Guide
Rev. 2.0 / December 6, 2013
Page 155 Figure 63: IDE 40 Pin and CompactFlash 50 Pin Connector

Chapter 3
Power and Reset

The information provided in this chapter includes:

3.1 ATX Style Power Control

3.2 Reference Schematics

Figure 35: AT and ATX Power Supply (1)

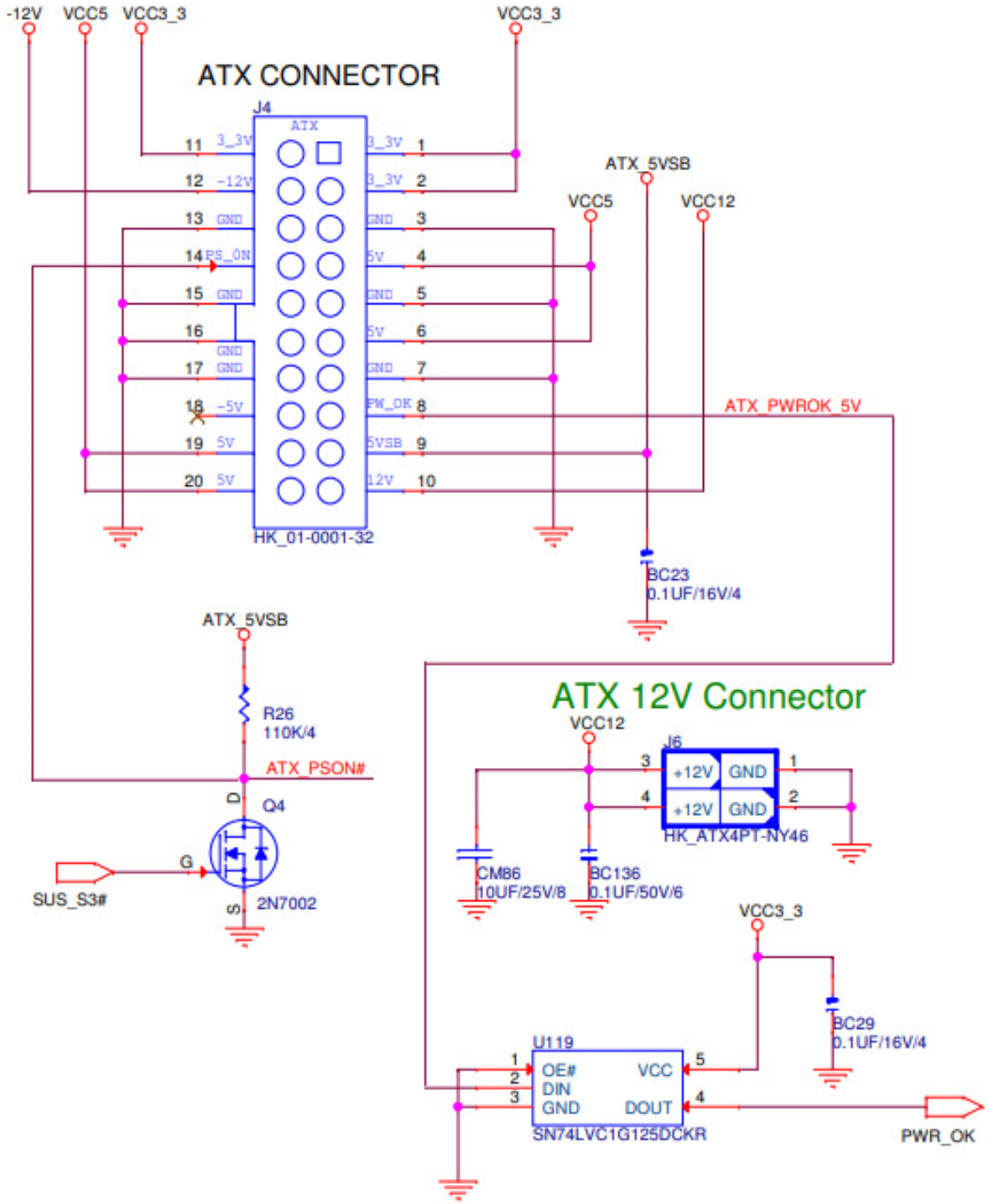


Table 26: ATX Signal Names

ATX Signal Name	Description
PS_ON#	Active-low, TTL-level input to ATX supply that, when low, enables all power rails. If high or floating, all ATX power rails are disabled except for the +5V Suspend rail.
PWR_OK	Active-high, TTL-level output signal from the ATX supply that indicates that the +12V, +5V, +3.3V and -12V outputs are all present and OK to use.
+12V1DC	+12V power rail for use by all system components except for the CPU, controlled by
+12V2DC	+12V power rail for use by the CPU, controlled by PS_ON#. This power rail appears on a separate 2x2 connector for CPU use only.
+5VDC	+5V power rail, controlled by PS_ON#
+3.3VDC	+3.3V power rail, controlled by PS_ON#
-12VDC	-12V power rail, controlled by PS_ON#
+5VSB	+5V Suspend power rail, present whenever the ATX supply is connected to its AC power input source.
COM	Common return path – usually referred to as “ground” or GND.

3.3 Routing Considerations

3.3.1 VCC_12V and GND

For the +12V power input (VCC_12V) to the Module, the trace should be wide enough to handle the maximum expected load. A power plane may be used for VCC_12V but is not recommended; VCC_12V should not be used as a reference for high-speed signals, such as PCIe, USB, or even PCI, because there may be switching noise present on VCC_12V.

A 40W CPU Module can draw over 3.5A on the VCC_12V pins. Sizing the VCC_12V delivery trace to handle at least twice the expected load is recommended. K eep the Carrier Board VCC_12 trace short, wide, and away from other parts of the Carrier Board.

If there are layer transitions in the power delivery path, use redundant “power” vias – vias that are sized with larger holes and pads than default vias. For the GND return, use a solid, continuous plane, or multiple planes, using the heaviest possible copper. Connect all available power and ground pins available on the COM Express Module to the Carrier Board.

3.3.2 VCC_5SBY Routing

The +5V Suspend power rail should be sized to handle 2A. Most Modules will use less than 2A for the \power rail. Modules with multiple Ethernet channels and wake-on-LAN capability will use more current. The COM Express Specification allows up to 2A on this rail.

Chapter 4
Carrier Board PCB Layout Guidelines

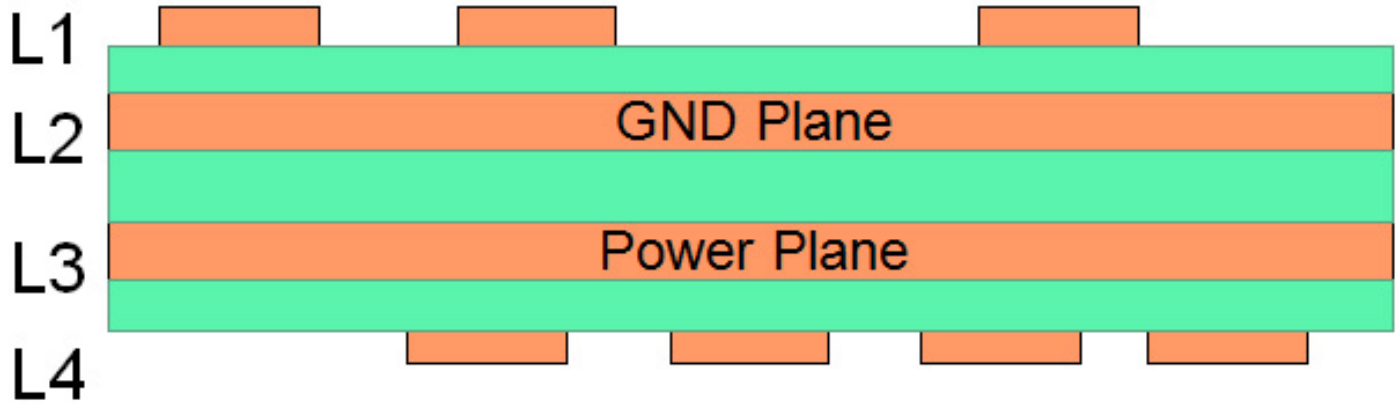
4.1 General

4.2 PCB Stack-ups

Note: 'Carrier Board PCB Layout Guidelines' assumes a thickness for the carrier PCB to be 0.0625 inches. Other PCB mechanics are possible but the described Stack-ups need to be adapted.

4.2.1 Four Layer Stack-up

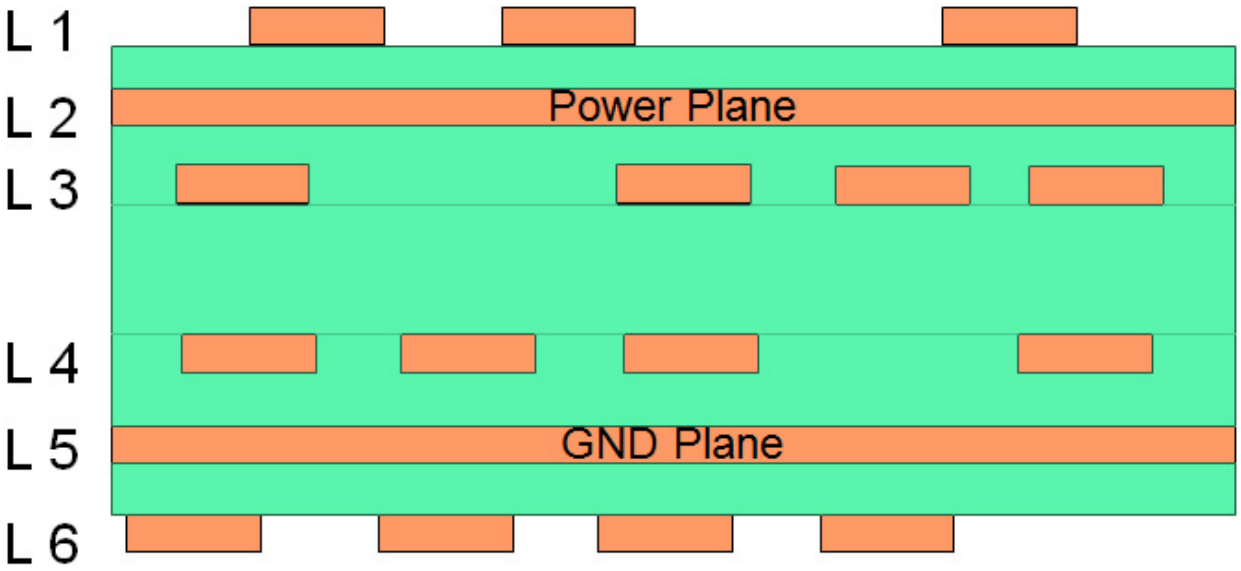
Figure 36: Four-Layer Stack-up



The figure above is an example of a four layer stack-up. Layers L1 and L4 are used for signal routing. Layers L2 and L3 are used for solid ground and power planes respectively. Microstrips on Layers 1 and 4 reference ground and power planes on Layers 2 and 3 respectively. In some cases, it may be advantageous to swap the GND and PWR planes. This allows Layer 4 to be GND referenced. Layer 4 is clear of parts and may be the preferred primary routing layer.

4.2.2 Six Layer Stack-up

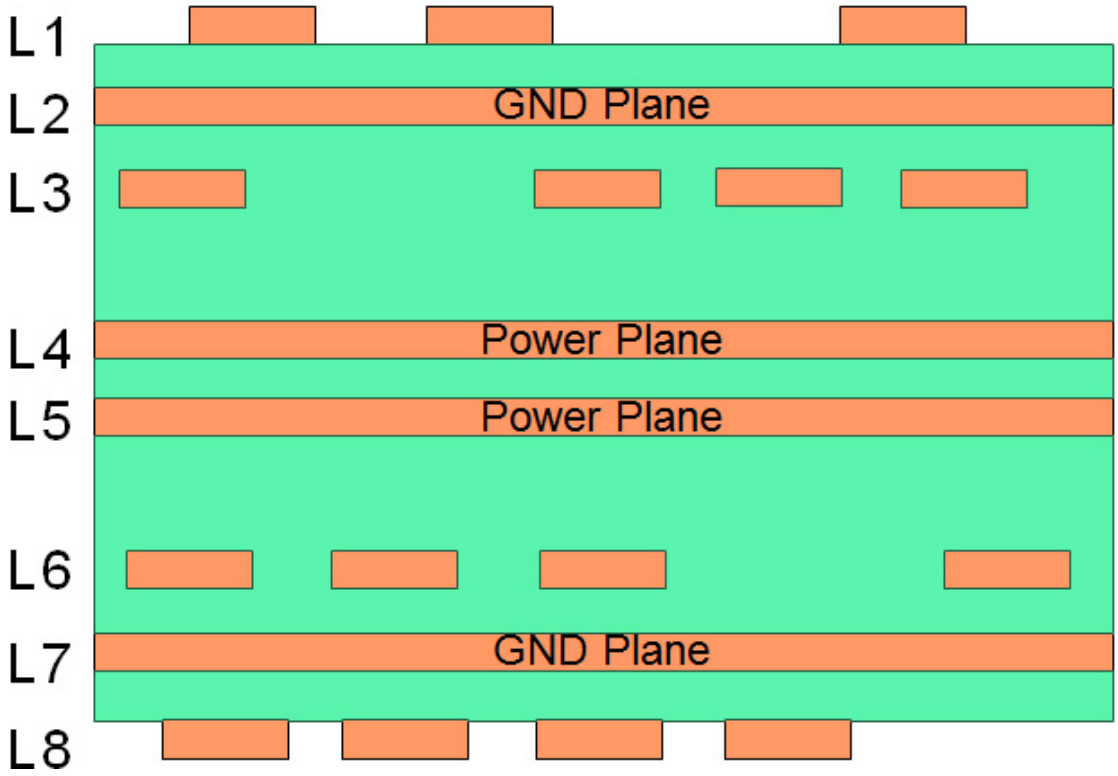
Figure 37: Six-Layer Stack-up



The figure above is an example of a six layer stack-up. Layers L1, L3, L4 and L6 are used for signal-routing. Layers L2 and L5 are power and ground planes respectively. Microstrips on Layers 1 and 6 reference solid ground and power planes on Layers 2 and 5 respectively. Inner Layers 3 and 4 are asymmetric striplines that are referenced to planes on Layers 2 and 5.

4.2.3 Eight Layer Stack-up

Figure 38: Eight-Layer Stack-up



The figure above is an example of an eight layer stack-up. Layers L1, L3, L6 and L8 are used for signal-routing. Layers L2 and L7 are solid ground planes, while L4 and L5 are used for power.
Microstrip Layers 1 and 8 reference solid ground planes on Layers 2 and 7 respectively.
Inner signal Layers 3 and 6 are asymmetric striplines that route differential signals.
These signals are referenced to Layers 2 and 7 to meet the characteristic impedance target for these traces. To reduce coupling to Layers 4 and 5, specify thicker prepreg to increase layer separation.

4.3 Trace Impedance Considerations

Figure 39: Stackup & Impedance

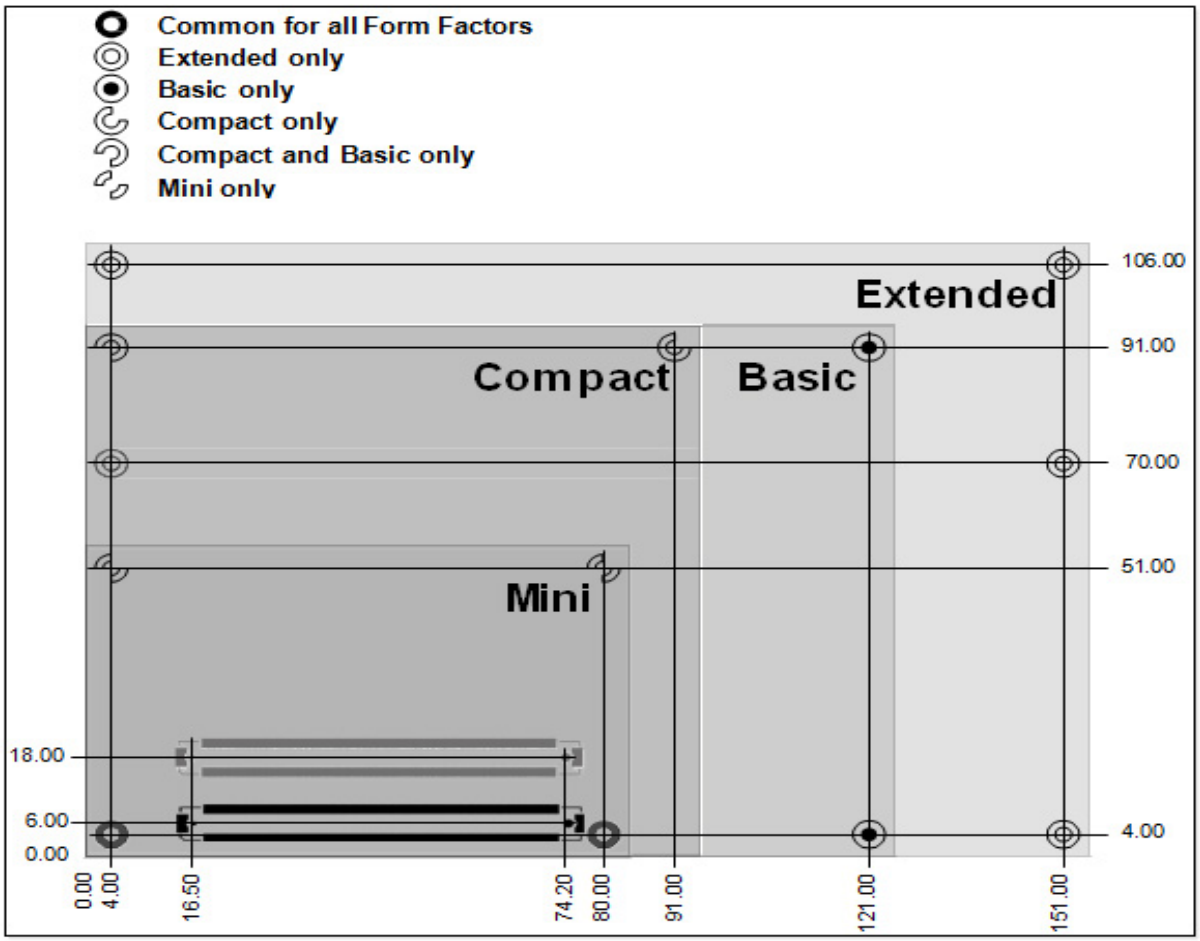
Layer		Glass Style & Cu Wt	Thickness
		Solder resist	0.8
Top		H OZ plate to 1OZ	1.4
	P.P	1080HR	2.8
L2		1 OZ	1.4
	core	FR-4 1.30 t	48.2
L3		1 OZ	1.4
	P.P	1080HR	2.8
Bottom		H OZ plate to 1OZ	1.4
		Solder resist	0.8
		Unit：	mil
		Total thickness	61

	Single End				Differential				
	27.4± 10%	37.5± 10%	40± 10%	50± 10%	80±10%	85±10%	86±10%	90±10%	100±10%
W / S	12.5	7.5	6.5	4	5 / 5	4 / 4.5	4 / 5	4 / 6.5	4 / 9
Ω	26.23	36.06	39.04	49.44	77.65	83.59	85.35	89.23	98.22
W/S	12.5	7.5	6.5	4	5 / 5	4 / 4.5	4 / 5	4 / 6.5	4 / 9
Ω	26.23	36.06	39.04	49.44	77.65	83.59	85.35	89.23	98.22

Chapter 5
Mechanical Considerations

5.1 Form Factors

Figure 40: Mechanical comparison of available COM Express Form Factors



All dimensions are shown in millimeters.

5.2 Heatspreader

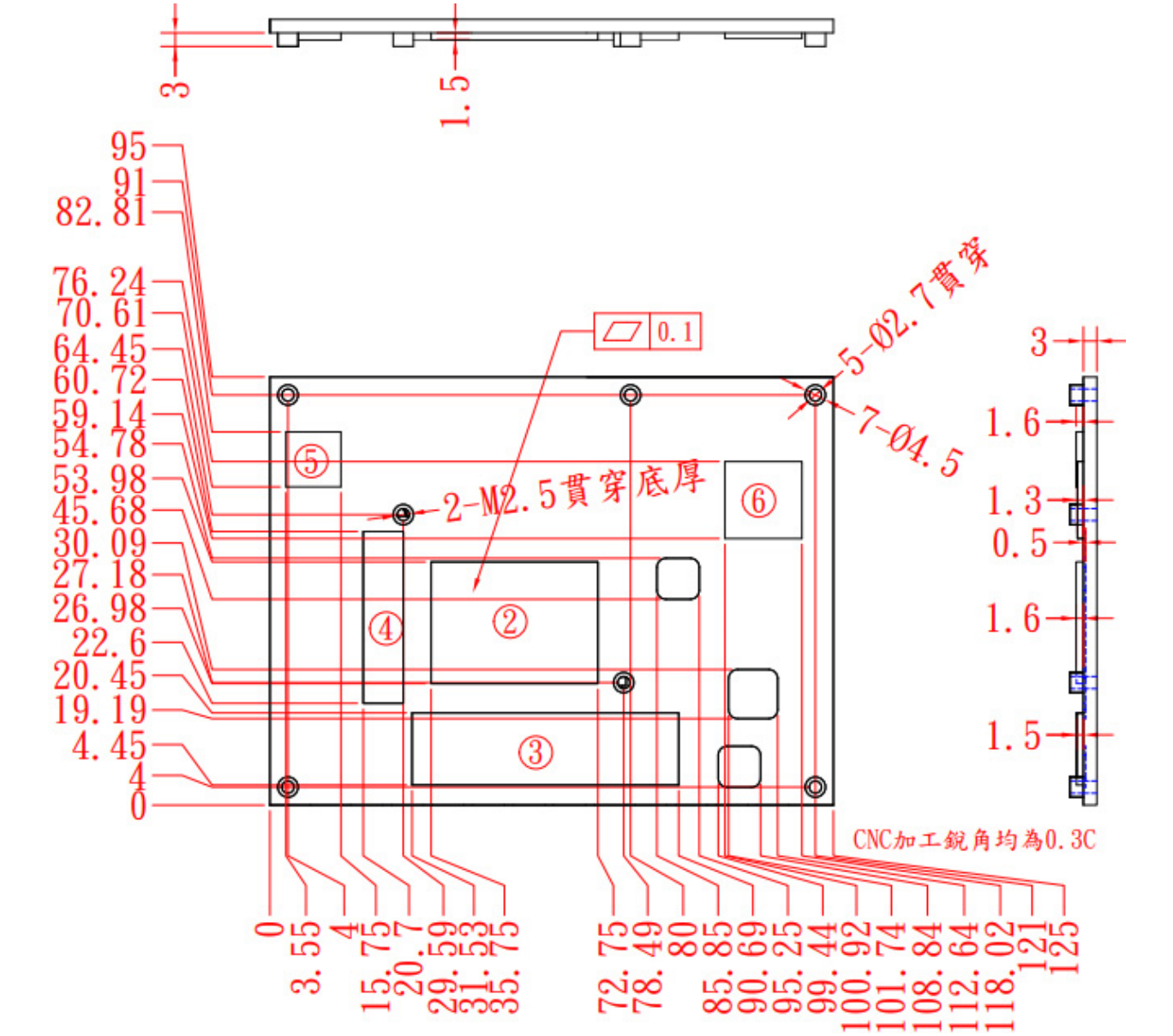


Figure 41: IBASE HSET976-1 Heatspreader

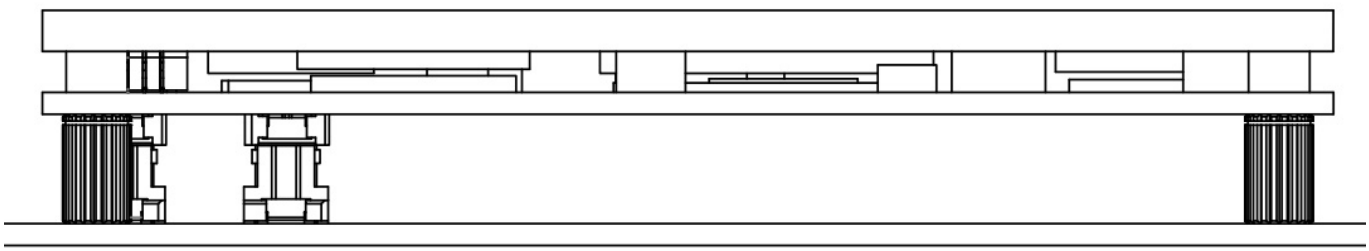


Figure 42: Side View of Heatspreader, COM Express Module & Carrier board layer.

5.3 COM Express Carrier Board

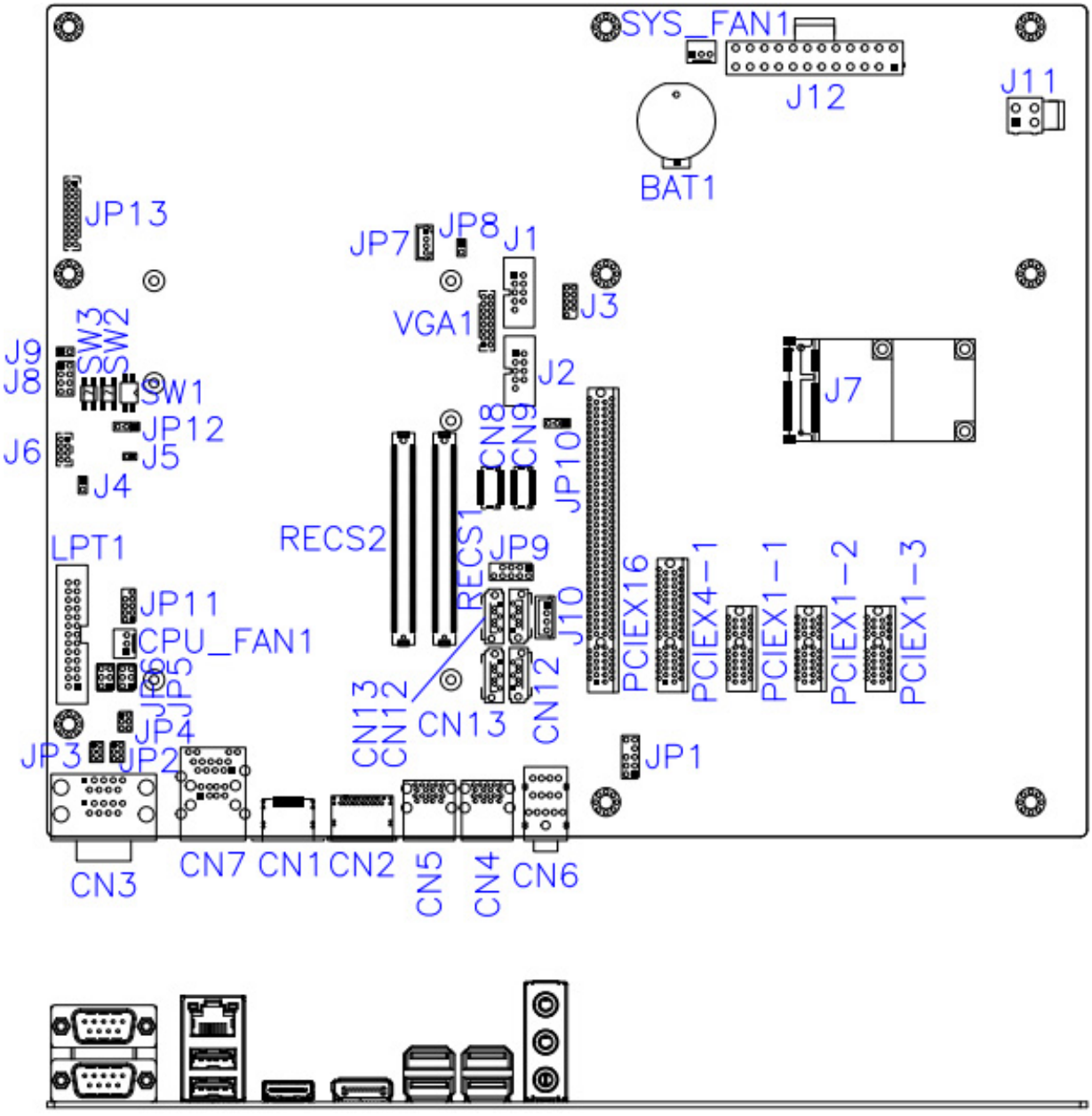


Figure 43: IBASE IP413 COM Express Carrier Board

5.4 COM Express Module and Heatsink

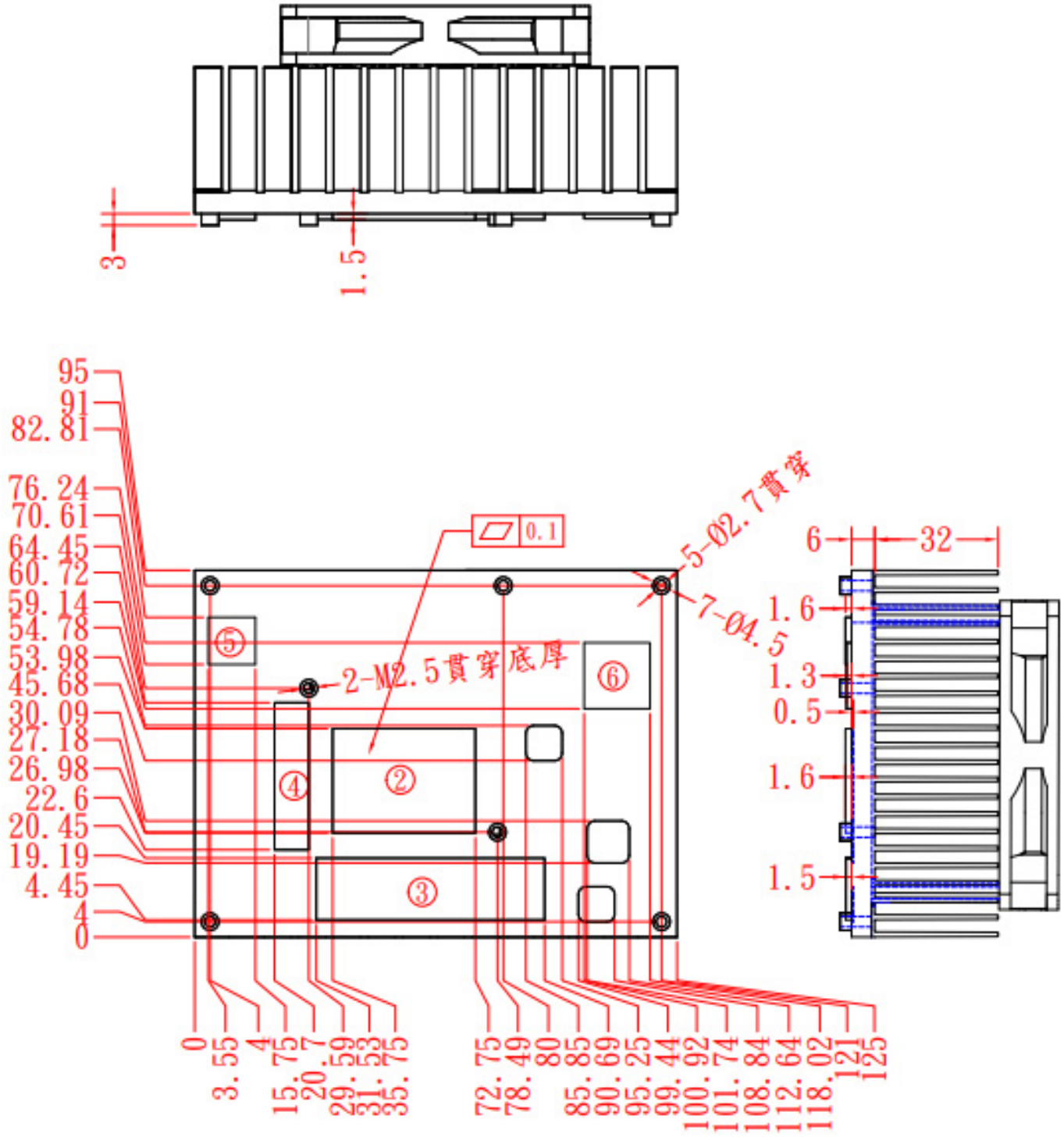


Figure 44: IBASE ET976 and Heatsink

5.5 COM Express Connector (Tyco)

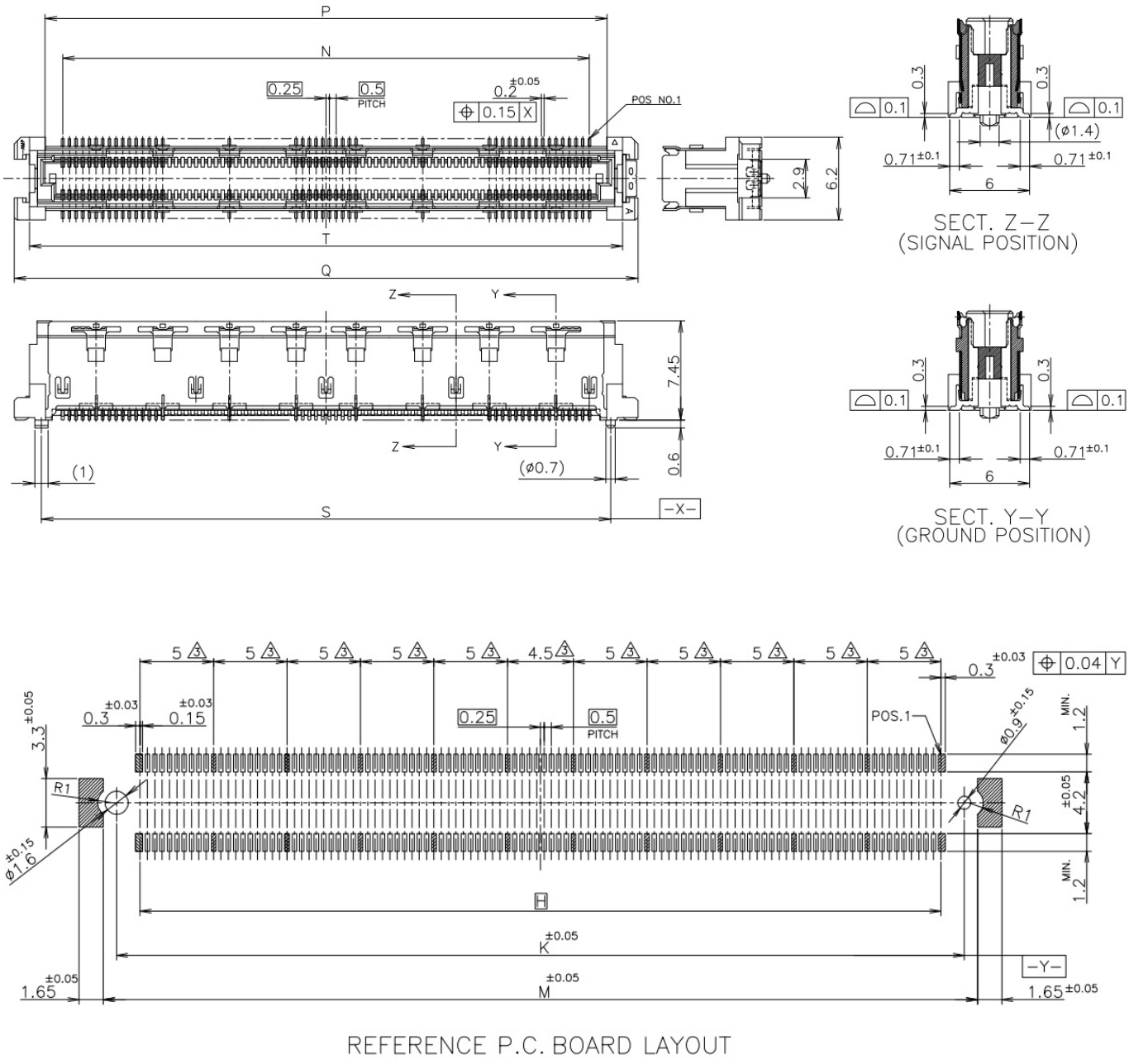


Figure 45: Tyco 220-pin COM Express Connector (Pitch 0.5mm, H: 8mm)